

CROSSVOLTTM Low Voltage Logic Series Databook

LCX Family
LVX Translator Family
LVX Bus Switch Family
LVX Family
LVQ Family
LVT Family

LCX family with 5 to legant inches and outputs
Introducing the and the grands fransceivers



CROSSVOLT™ LOW VOLTAGE LOGIC SERIES

DATABOOK

1994 Edition

National®

SE/167M	PLANTM
SE327M	PLANATM
SOPLANARTM	PLAYER
SOPLANAR-ZTM	PLAYER + TM
LERICTM	Polycraft TM
MACMOSTM	POLYC

Description and Family Characteristics

Ratings, Specifications and Waveforms

Quality and Reliability

Application and Design Considerations

LCX Family

LVX Translator Family

LVX Bus Switch Family

LVX Family

LVQ Family

LVT Family

Physical Dimensions

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No		16	X	×	×		*	16374	16-8it D
									Latches
Broadside Pin Out	TRI-STATE	Enable (Level)		TVJ	KOL		LVO	Туре	Function/Description
No		1 (H)		×	- ×	X	X	378	Octal Transparent Latch
Yes	seY	(L)	8			×	×		Octal Transparent Latch
No		2 (H).	16	×				16373	16-Bit Transparent Latch
								vers	Buffers/Line Dri
Inverting/ Non-Inverting	elda (leva		TVJ	LCX	KVJ	DVJ		Туре	Function/Description
	(J)		×			×		125	Quad Buffer
	(1)		×		×			240	Octal Buffer/Line Driver
	(H)++					×		241	Octal Buffer/Line Driver
M	(L)			×	×	×		244	Octal Buffer/Line Driver
1	(J)		×					18240	16-Bit Buffer/Line Driver
N	(4)			×		1		16244	16-Bit Buffer/Line Driver



Low Voltage Logic Selection Guide and the second of the se

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Gates

Function/Description	Туре	LVQ	LVX	LCX VW	LVT
Quad 2-Input NAND	00	PLST XTE Output	Talina Xhag h	w voltage utilate	741 VX19E LU
Quad 2-Input AND	08	nave X oiilume	8 Decxider/D	ow Voltage 1-of	74LVX138 L
Quad 2-Input OR	32	x rexeld	d 2-In x ut Mult	ow Voltage Qua	74LVX157 L
Quad 2-Input NOR	02	n Mas x Reset.	D Flipx Flop wi	ow Voltage Hex	74LVX174 L
Quad 2-Input Exclusive-OR	86	O LOT A X	OFFICE STATES	ow Voltage Dela	ALVAZAU L
Hex Inverter	04	TranscXsiver	BidiiXctional	ow Voltage Octa	74LVX245 L
Hex Schmitt Trigger Inverter	14		doll-ixil-Flop	ow Voltage Octa	74LVX273 L

74LVX373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs 8-56 74LVX374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs SQ017-qi17

Function/Description	Туре	LVQ	LVX	LCX	LVT	Data Inputs	TRI-STATE® Outputs	Master Reset
Dual D TATE	74	X	X	i analio\	aldaun	2	No s and	No
Hex D	174	x	X			6	metay No's tol a	Yes
Octal D TATE	273	visognati	nterix ce	/oltage la	gurable	uppl8 Conf	245 8-6N Dual S	Yes
Octal D	374	×	×	x	× × ×	8	Yes	No
16-Bit D	16374			х	x	16	Yes	No

Latches

Function/Description	Туре	LVQ	LVX	LCX	LVT	Data Inputs	Enable (Level)	TRI-STATE® Outputs	Broadside Pin Out
Octal Transparent Latch	373	×	×	×	×	8	1 (H)	Yes	No
Octal Transparent Latch	573	×	X			8	1 (L)	Yes	Yes
16-Bit Transparent Latch	16373			×	Х	16	2 (H)	Yes	No

Buffers/Line Drivers

Function/Description	Туре	LVQ	LVX	LCX	LVT	Enable (Level)	Inverting/ Non-Inverting
Quad Buffer	125	х	x		×	4 (L)	N
Octal Buffer/Line Driver	240	x	x	x	x	2 (L)	1
Octal Buffer/Line Driver	241	x				1 (L) + 1 (H)	N
Octal Buffer/Line Driver	244	x	x	x	x	2 (L)	N
16-Bit Buffer/Line Driver	16240			X	х	4 (L)	1
16-Bit Buffer/Line Driver	16244			x	х	4 (L)	N

Decode	ers/De	multip	olexers
--------	--------	--------	---------

Function/Description	Туре	LVQ	LVX	LCX	LVT	Enable (Level)	Active Address Inputs	Outputs
1-of-8 Decoder/Demultiplexer	138	х	x	1 1 2		2 (L) + 1 (H)	3	8

Multiplexers

Function/Description	Туре	LVQ	LVX	LCX	LVT	Enable (Level)	True Output	Complement Output
8-Input Multiplexer	151	x				1 (L)	Yes (1)	Yes (1)
Quad 2-Input Multiplexer	157	x	x			1 (L)	Yes (4)	No

Transceivers/Registers

Function/Description	Туре	LVQ	LVX	LCX	LVT	Registers	Enable (Level)	TRI-STATE® Outputs
Octal Bidirectional Transceiver	245	х	х	х	х	No	1 (L)	Yes
Octal Bus Transceiver and Register	646			X	X	Yes	1 (L)	Yes
Octal Bus Transceiver and Register	652			х	х	Yes	1 (L) + 1 (H)	Yes
16-Bit Bidirectional Transceiver	16245			Х	Х	No	2 (L)	Yes
16-Bit Bus Transceiver and Register	16646			х	х	Yes	2 (L)	Yes
16-Bit Bus Transceiver and Register	16652			x	x	Yes	2 (L) + 2 (H)	Yes

Translators

Function/Description	Туре	LVQ	LVX	LCX	LVT	TRI-STATE® Outputs	3V or 5V Configurable I/O	V _{CCA}	V _{CCB}
Octal Translating Transceivers	3245		х			Yes	No	2.7V-3.6V	4.5V-5.5V
Octal Translating Transceivers	4245		х			Yes	No	4.5V-5.5V	2.7V-3.6V
Octal Translating Transceivers	C3245		х		17	Yes	Yes	2.7V-3.6V	3.0V-5.5V
Octal Translating Transceivers	C4245		х			Yes	Yes	4.5V-5.5V	2.7V-5.5V

Bus Switches

Function/Description	Туре	LVQ	LVX	LCX	LVT	TRI-STATE® Outputs	3V or 5V Configurable I/O	Vcc
10-Bit Bus Switch or 5-Bit Bus Exchanger	3L383		х			Yes	Yes	4.0V-5.0V
10-Bit Bus Switch	3L384		x			Yes	Yes	4.0V-5.0V

						Active	
Function/Description	OVJ	XVJ	KOJ	TVJ	Enable (Level)	Address	Outputs
of-8 Decoder/Demultiplexer		X			2 (L) + 1 (H)		8

Complement	True	eldsn3	LVI	LCK	LVX	LVQ	Type	Punction/Description
Yes (1)	Yes (1)	(L)				X		8-Input Multiplexer
No		1 (L)					167	

Transceivers/Registers

TRI-STATE Ouiputs	Enable (Level)	Registers	LVY	LCX	XVJ	DVJ	Туре	Function/Description
	1 (L)	No	×	×		X	245	Octal Bidirectional Transceiver
	(J) 1			×			848	
	1 (L) + 1 (H)		×	X				Octal Bus Transceiver and Register
Yes		No		×				16-Bit Bidirectional Transcalver
				×				
89Y	2(L) + 2(H)			×				16-Bit Bus Transceiver and Register

Translators

Vcca	Voca	8V or 6V Configurable I/O	PRINSTATE® Outputs	LVT	XAT	LVQ	Type	Function/Description
4.5V-5.5V	V0.8-V7.S	No			×		3245	Octal Translating Transceivers
2.7V-3.6V	4.5V-5.5V	No			×			
	2.77-3.67	Yes	seY		×		C3245	
2.7V-5.5V	4.5V-5.5V	Yes			×		C4245.	Octal Translating Transceivers

	3V or 5V Configurable 1/O	TRI-STATE* Outputs	LVT	KOJ	XVI	LVQ	турв	Function/Description
		Yes			×			10-Bit Bus Switch or 5-Bit Bus Exchanger
4.0V-5.0V		Yes					31384	10-Bit Bus Switch



-		25v v.		atto
		70. 57	JEG. 103	
		Life 3	8.0%	0.17 (C.)16

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Description and Family Characteristics

Dual Supply

Introduction

In order to provide optimum logic solutions for a variety of low voltage applications, National Semiconductor offers several low voltage logic product families. Each of these families possess a unique set of features and operating characteristics optimized for a particular low voltage application. All National low voltage logic devices share the following features:

- low or "zero" static power dissipation (<100 nA typical for LVQ)
- reduced dynamic power consumption
- lower switching noise than comparable higher supply voltage counterparts
- compliance with EIA-JEDEC low voltage interface standard #8-1B

Output drive, translation capabilities, switching speed and interface flexibility are examples of the characteristics that differentiate these low voltage logic families.

Family Specifications

To assist the designer in selecting one of National Semiconductor's Low Voltage Logic families the specifications for a '245 function are compared below for easy reference. Please reference individual data sheets for specific device information.

DC Electrical Characteristics

Recommended Operating Conditions

Information)	(Visinniary)	Switches	LVX	XVJ			LVT
'24S	LVQ	LVX 0.25	Dual Supply Translating Transceivers	Bus Switches	8,0	LCX (Preliminary)	(Advance Information)
4	'245	'245	4245	3L383	3.0	'245 xsM	'245
Supply Voltage (V _{CC})	2.0V to 3.6V	2.0V to 3.6V	2.7V to 3.6V	4.0V to 5.5	8.5V	2.0V to 3.6V	2.7V to 3.6V
5.5	8.5	8.6	and 4.5V to 5.5V	16.5	3.5	r xsM	Тегн
Input Voltage (V _I)	0V to V _{CC}	0V to 5.5V	0V to 5.5V	0,91	01	0V to 5.5V	0V to 5.5V
Output Voltage (VO)	0.1	6.6	N. C.	14.0	C.	XERVI	2741
Active	0V to V _{CC}	0V to V _{CC}	0V to V _{CC}	3.6	.5	0V to V _{CC}	OV to VCC
TRI-STATE®	0V to V _{CC}	0V to V _{CC}	0V to V _{CC}	1.5	.5	0V to 5.5V	0V to 5.5V
Operating Temperature (T _A)	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +8	35°C	-40°C to +85°C	-40°C to +85°C
Input Rise and Fall Time	125 mV/ns	0 ns/V to 100 ns/V	8 ns/V			10 ns/V	10 ns/V

DC E	Electr	ical Charact	eristics			lenoth	CHINA
				LVX		refoubnesi	mos LVT
		LVQ	LVX	Dual Supply Translating Transceivers	Bus Switches	LCX (Preliminary)	(Advance Information)
		'245	'245	4245	'3L383	'245	'245
VIH	Min	2.0V	2.0V	2.0V	2.0V	2.0V	2.0V
V _{IL}	Max	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
Voh	Min e2 Isnotl	2.48V @ I _{OH} = -12 mA	2.48V @ I _{OH} = -4 mA	3.76V @ I _{OH} = -24 mA	utions for a vi	2.2V @ I _{OH} = -24 mA	$2.0V @ I_{OH} = -32 \text{ m/s}$
V _{OL}	Max	0.44V @ I _{OL} = +12 mA	0.44V @ I _{OL} = 4 mA	0.44V @ I _{OL} = 24 mA	milies. Each o atures and o	0.55V @ I _{OL} = 24 mA	0.55V @ I _{OL} = 64 mA
I _{IN}	Max	±1.0 μA	±1.0 μA	±1.0 μA	±1 μA	±5.0 μA	±10 μA
Icc	Max	40 μΑ	40 μΑ	80 μΑ	3 μΑ	10 μΑ	:891112 mA
loz	Max	±3.0 μA	±2.5 μA	±5 μA	±1 μA	Au 6±	±1 μΑ
VOLP	Max	0.8V	0.8V	1.5V/0.8V	noi	0.8	TBD
V _{OLV}	Min	-0.8V	-0.8V	-1.2V/-0.8V	arable higher	g noise 8.0an com	niriotiwa TBDol
V _{IHD}	Max	2V	2V	2V	-1	rparts	TBD TBD
V _{ILD}	Max	0.8V	0.8V	0.8V	onege menat	WOLOGOGOWA W	TBD

AC Electrical Characteristics

				LVX			13/7
TVJ	хээ	LVQ	LVX	Dual Supply Translating Transceivers	Bus Switches	(Preliminary)	(Advance Information)
(Advance	Units = ns	9) '245	245	4245	'3L383	'245	'245
T _{PHL}	Max	10.5	11.5	arevi 8.5 arT	0.25	7	4
TPLH	Max and	10.5	11.5	48.5	0.25	847	4
TpzLot V	Max of V0	3 13.5 Va	16.5	2.7Ve33.6V	Va.8 6.5/0.9	Va.c 8.50.s	Supply \2.8age (Voc)
T _{PZH}	Max	13.5	16.5	9.5	6.5	8.5	5.5
T _{PHZ}	Max	15	14.5	8.5	5.5	7.5	5.9
T _{PLZ}	Max	15	14.5	7	5.5	7.5	4.8
TOSHLY	Max v of v	1.5	1.5	2015/0	coV of VO	20 V cl V0	1 avitoA
Toslh	Max 3 of V	1.5	1.5	00V1.5V0	OV to Voc	00 V of V0	TRI-STATE®
40°0°10 + 85	- 0°68+ of 0°	85°C - 40	- 40°C to +	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	Operating Temperature (T _A)
V\en 01	10 ns/V			V\sn 8	0 ns/V to	125 mV/ns	Input Rise and Fall Time

Operating Voltage Features of National Semiconductor's local against wolling Low Voltage Logic Families

One of the most popular uses of low voltage logic is for translation between voltage levels, '244 and '245 functions are most often used for translation, but other functions are also used. The following table summarizes the translation capabilities for each family.

April Recorded Street Co.		Mixed		Translators	the should be a second	Mixed	Mixed
Parameter	Pure 3V	Voltage Tolerant	Configurable	Configurable	Conditional (Note 1)	Voltage Tolerant	Voltage Tolerant
	LVQ	LVX	LVX3245/4245	LVXC3245/4245	LVX3L383/4	LCX	TVI
VCC SOV	2.0V-3.6V	2.0V-3.6V	es yes	yes)	4.0V-5.5V	2.0V-3.6V	2.7V-3.6V
V _{CCA}		yes	4.5V-4.5V or	2.7V-3.6V or	yes	164	Zero Static Po
yes		yes	a 2.7V-3.6V	4.5V-5.5V	yes		Low EMI
V _{CCB} sev	1	yes	4.5V-5.5V or	2.7V-5.5V or	yes	Am (atchup > 300
			2.7V-3.6V	3.0V-5.5V		901	Alternative So
Inputs	3V	Accepts 3V and 5V	0V-V _{CC}	0V-VCC	0V-V _{CC}	Accepts 3V and 5V	Accepts 3V and 5V
I/O and Outputs	3V	3V Only	ON-V _{CC}	0V-V _{CC}	Interfaces with 3V/5V	Accepts 3V and 5V (Note 2)	Accepts 3V and 5V (Note 2)
A-Port		ува	Interfaces with 3V or 5V	Interfaces with 3V or 5V	sey	Pin	Corner Supply
			(Fixed)	(Fixed)			Product Range
B-Port		yae yae	Interfaces with 3V or 5V (Fixed)	Interfaces with 3V or 5V (Configurable)	yes yes no		Castes/Mol Ocials 10-Bit

Note 1: Translation feature implemented by adding a diode between V_{CC} and the device.

Note 2: Only when outputs in TRI-STATE condition (when an I/O is an input it can accept a 5V stimulus).

All the families except LVQ provide some sort of translation capability. LVX and LCX will accept 5V signals on the inputs, and LCX will also tolerate 5V signals on the outputs when the outputs are in TRI-STATE. The LVX3L383/4 devices can be used as "zero delay" translators when a diode is used between V_{CC} and the devices. For pure translation,

the LVX Dual Supply Translating Transceivers are unsurpassed. They can even be used to drive 5V CMOS inputs and the LVXC3245/4245 devices have B-port I/O which can be configured for 3V or 5V "on the fly". For further information on interfacing National Semiconductor's Low Voltage Logic to 5V Logic families see Section 4.

Offerings and analysis and

and the LVXG8245/4245 devices have B-port I/O which can be configured for 3V or 5V "on the fly". For further information on interfacing National Semiconductor's Low

			LVX	aeilin	ge Logic Fal	LVT
45 func apure most	ge level of LVQ Menizes the translate	wing xv) e sum	Dual Supply Translating Transceivers	Bus Switches	(Preliminary)	(Advance Information)
Translation (5V ←→ 3V)		eroiste	1017		Mixed	
Input Bidirectional	TO HOMOTON	yes	yes yes	yes yes	yes yes	yes
Configurable	AN no ISXVI	no	yes	no	XVI no OVI	no
V _{OLP} < 0.8V	yes vo A	yes	yes	yes	e_vosyes va.e_v	yes yes
Zero Static Power	yes	yes	yes way	yes	yes	no no
Low EMI	yes	yes - V	yes Va.	yes	yes	yes
Latchup > 300 mA	yes	yes	yes to Va	a-Vayes	yes	yes sooV
Alternative Source Available	yes	yes	yes	yes	atgeoo / yes	yes
Power Up Output Hi-Impedance	no	no	no	no	no no	yes
Power Down Output Hi-Impedance	Valve driv	no no	no oo	/~V0 no	yes VE	yes
Corner Supply Pin	yes	yes	yes 290	yes	yes	yes
Product Range Gates/MSI Octals 10-Bit 16-Bit	yes yes no no	yes yes no	no yes no no (b	no no ves no	no yes no yes	no yes no yes
Current Package	SOIC, EIAJ, QSOP-Octals Only	SOIC, EIAJ, SSOP I	SOIC, QSOP	SOIC, QSOP, TSSOP	SOIC, EIAJ, TSSOP,	SOIC, EIAJ, TSSOP,

SSOP-16-Bit Only SSOP-16-Bit Only

and LCX will also tolerate 5V signals on the outputs when the outputs are in TRI-STATE. The LVXSL383/4 devices can be used as "zero delay" translators when a diode is used between $V_{\rm CC}$ and the devices. For pure translation,

Switching Induced Noise

Process Technology

A wide range of processing technologies are used to manufacture the various low voltage product families. Process selection is based upon the conversion of product electrical features to technological demands at the device level. Table I summarizes the process characteristics by product line.

	ryjabi «	and ids[P2]	[[N] ≥ Ids[N]]	LVX	he net result is th	OLP and Voty.		
Product Li	ne	LVQ	LVX	Dual Supply Translating Transceivers	Bus Switches	stitenLCXsion e	are must be tale tine TV1 rs if the compressed swit low-voltage-tur	gallov Units
Process	P2-T	1.5 CMOS	1.0 CMOS	0.8 CMOS	1.0 BICMOS	0.8 CMOS	1.0 BICMOS	tor's p
Device Characte	eristics		14	-in	d maximum spec	only guaranteed	vith the industry's	along v
TOX	nom	225	150	150	150	150	150	A A
Abs Max V _{CC}	max	7.0	7.0	7.0	oitem 7.0e and	ctional 0.7 correct	ruit a a7.0 peb t	Viure
LEFF NMOS	nom	1.05	0.65	0.6	0.65	0.6	0.65	μm
LEFF PMOS	nom	1.05	1.0	0.75	fluor 0.7 th noit	and 0.75 I-deli	tuqtuc0.7s to ea	so µm
BNPN	nom	n/a	n/a	n/a	n/a	n/a	ent of 190 hoods	haves
Process Charac	teristics		1		torrough and analo		OMOTPIGMOO I	A 19733AZ
Starting Materia	al.	P-eni on	P-eni on	N-eni/N++	N-eni/N++	N-eni/N++	N-eni/N++	20.4.22.62

Starting Material	P-epi on P++	P-epi on P++	N-epi/N++	N-epi/N+++	N-epi/N++	N-epi/N++	lgV •
Minimum Feature	stoold ¹ .4 entre	1.0	0.8 as	musas)1;0= [99	abi = 0,8 jabi «	- vo =1.039, [9]	byμm
M1 Pitch min	(slab 4.5 8 br	A 3.500 18	2.0	3.5	2.0	sol evita.5 las via	μm
M2 Pitch min	6.0	5.0	2.5	5.0	2.5	5.0	μm

Switching Speed and Static Output Drive of GERRARD YLDAMRETXE BRA & DIA A REGOM

National Semiconductor offers the low voltage system designer choices when it comes to switching speed, output drive and mixed supply level flexibility. Table II summarizes the performance of the various low voltage logic families with regard to these system critical parameters.

TABLE II

	of the circuit I	description i	be LVX d b	N1 saturates an	ov = [III] = Vo	S(N1) = Vcc. V	o V
Parameters	LVQ	LVX	Dual Supply Translating Transceivers	Bus Switches	LCX	(Advance Information)	Units
T _{PD} (3.0V, 85°C)	9.5	12.0	9.0	250 ps (Note 1)	6.5	4.0	ns
I _{OL} (Note 2)	12	4	24	n/a	24	64	mA
I _{OH} (Note 3)	-12	-4	-24	n/a	-24	-32	mA
Abs Max V _{CC}	7	7	7	7	7	7	٧
Maximum V_{IH} ($V_{CC} = 3.0V$)	V _{CC} + 0.5	5.5	V _{CC} + 0.5	5.5	5.5	5.5	٧
Maximum V_{OH} ($V_{CC} = 3.0V$)	V _{CC} + 0.5	V _{CC} + 0.5	V _{CC} + 0.5	5.5	5.5 (Note 4)	5.5 (Note 4)	٧

Note 1: Calculated based upon 50 pF load and 5Ω nominal channel resistance

Note 2: Refer to individual datasheets for VOL level.

Note 3: Refer to individual datasheets for $V_{\mbox{OH}}$ level.

Note 4: V_{OH} is permitted to rise above V_{CC} only when OEb $\geq V_{IH}$.

Switching Induced Noise

Reducing the power supply potential and compressing the output swing of a high drive output buffer reduces the switching induced noise that it propagates or generates. At the same time using advanced technology to provide aggressive propagation delay and large load driving capabilities serves to increase V_{OLP} and V_{OLV}. The net result is that great care must be taken in the design of high speed, low voltage line drivers if the noise benefits of the reduced supply and compressed swing are to be preserved. By incorporating a low-voltage-tuned version of National Semiconductor's proven Graduated Turn-On (GTOTM) circuitry (Note 1), best-in-class propagation delay guarantees are achieved along with the industry's only guaranteed maximum specifications for ground bounce, undershoot and dynamic input thresholds.

Figure 1 depicts a functionally correct, but schematically simplified representation of the National Semiconductor GTO circuit used throughout the low voltage portfolios. In the case of an output high-to-low transition this circuit behaves according to the following flow.

Note 1: United States Patents #4,961,010, #5,036,222 and #5,081,374

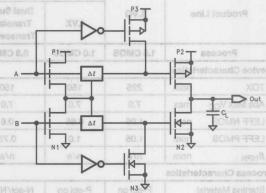
INITIAL CONDITIONS

- Vg[P1] and Vg[P2] are discharged to ~ 0V
- $Vgs[P1,P2] = V_{CC}$
- Vds[P1,P2] = 0V → Ids[P1] = Ids[P2] = 0 (assumes purely capacitive load)
- Vgs[N1] and $Vgs[N2] = 0V \rightarrow Ids[N1] = Ids[N2] = 0$
- \bullet V_O = V_{CC}

NODES A AND B ARE EXTERNALLY CHARGED TO V_{CC} FROM 0V

- Vg[P1,N1] rises to V_{CC}
- The Δt circuits delay the delivery of the signals A and B to P2 and N2
- Vgs[P1] = 0V, Ids[P1] = 0 → P1 is off
- Vgs[N1] = V_{CC}, Vds[N1] = V_{CC}, N1 saturates and begins to discharge C_L

- The Δt circuits now pass the signals at A and B
- Vgs[P2] = 0V, lds[P2] = 0 → P2 is off
 - Vgs[N2] = V_{CC}, Vds[N2] = V_{CC}, N2 saturates and discharges C_L
 - Ids[N2] > Ids[N1] and Ids[P2] > Ids[P1]



TL/F/12027-1

FIGURE 1. Simplified Schematic of GTO Noise Control

The connectivity within the Δt blocks is such that all signals arriving at nodes A and B are delayed en route to P2 and N2. This would serve to degrade the disable time performance of the buffer. N3 and P3 restore the disable time performance by bypassing the delay elements during LZ or HZ output transitions only. The turn-off signals to N2 and P2 are thereby delivered without delay.

Low Voltage Product Summaries

To assist the system designer in understanding the specific operating characteristics of each of the various products a brief description of the circuit topology for each is presented.

	(Advance (Information)		Bus Switches	Translating Transceivers	LVX	043	Parameters
			250 ps (Note 1)				T _{PD} (3.0V, 85°C)
					4	12	(OL (Note 2)
		-24		-24	> -	-12	
			7	7			
V				V _{CC} + 0.5	5.5		Maximum V _{IR} (V _{CC} = 3. 0V)
		5.5 (Note 4)	5.5		V _{CC} + 0.5	$V_{\rm GC} + 0.5$	Maximum VOH (VCC = 3.0V)

LVQ—Low Voltage Quiet CMOS Logic

The LVQ product line is targeted for 3.3V-only applications where interfacing to 5V or other interface levels is not a requirement. Figure 2 depicts the circuitry common to the LVQ family. Complementary diode input protection is used but without the usual current limiting input resistor. This dramatically reduces the forward resistance associated with these junctions and significantly improves their input overshoot and undershoot clamping capabilities. Diode D1 protects the input node from positive voltage ESD events by conducting the charge to the V_{CC} node and away from the ESD sensitive structures internal to the device. D1 becomes forward biased when charge builds up on the input node such that the potential difference across D1 is larger than V_F for D1. This type of input protection circuit precludes the application of input signals containing components that rise above V_{CC} by more than the V_F of D1.

The complementary MOS output drivers used throughout the LVQ family include drain isolation junctions D5 and D6 that are reverse biased during normal operation. This implies that signals applied to any LVQ output node must not rise above $V_{\rm CC}+V_{\rm F}[{\rm D5}]$ or below GND $-V_{\rm F}[{\rm D6}]$. Operation outside this range will forward bias D5 or D6 and thus creating an undesirable forward conducting path to $V_{\rm CC}$ or ground. This current may result in violation of the Absolute Maximum Ratings for these devices which in turn may adversely and permanently affect device performance and reliability.

LVX-Low Voltage CMOS Logic

(with 5V Tolerant Inputs)

LVQ devices include output drivers that feature National Semiconductor's GTO noise control circuitry. The output transistors are designed with suitable dynamic current sourcing and sinking capabilities to assure incident wave switching when driving non-terminated transmission lines having a characteristic impedance of 750Ω or greater.

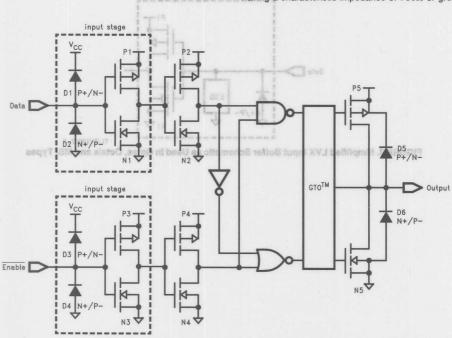


FIGURE 2. Simplified LVQ Schematic Diagram

TL/F/12027-2

LVX—Low Voltage CMOS Logic (with 5V Tolerant Inputs)

The LVX family is made up of three product groupings, each possessing a unique set of interfacing capabilities and characteristics optimized for specific applications.

- Gates, octals and MSI types being a single taril solid
- Dual Supply Translating Transceivers
- Bus Switches

The LVX gates, octals and MSI types all feature an alternate input ESD protection scheme that permit their inputs to receive signals whose logic-high levels exceed the supply voltage. Figure 3 shows a simplified LVX input buffer schematic that includes the alternate ESD structure.

Since there no longer exists a forward junction between the data input pin and V_{CC} the conduction path between the

data pin and V_{CC} is disrupted. The positive voltage limitation on the input pins increases from $V_{CC}+V_F$ to the minimum breakdown path tied to the input. For the LVX family of gates, octals and MSI products this value (BVDSS) is in excess of 7V. As in the case of LVQ products, LVX utilizes complementary MOS devices in its output stage and therefore cannot tolerate signals applied to its outputs outside the range defined by GND — V_F and $V_{CC}+V_F$.

LVQ-Low Voltage Quiet CMOS

The output drive available from LVX is scaled to provide the lowest possible dynamic power dissipation and leakage. By virtue of their pin capacitance specifications, low noise and high speed, LVX products are ideally applied in 3.3V battery powered systems where system performance requires 5V FACT propagation delays.

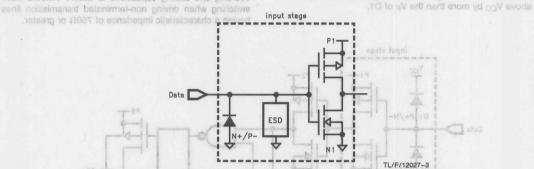
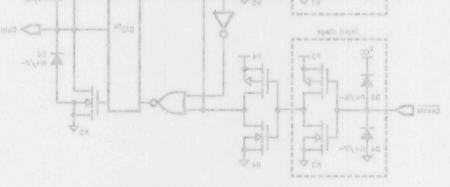


FIGURE 3. Simplified LVX Input Buffer Schematic as Used in Gates, Octals and MSI Types



PIGURE 2. Simplified LVQ Schematic Diagram

LVX—Low Voltage Dual Supply CMOS Translating Transceivers

The LVX family of true translating transceivers use an entirely different approach to the mixed supply interfacing issue. Not just overvoltage tolerant, these devices are true translators—meaning that they receive 3V signals and output 5V signals, and receive 5V signals and output 3V signals. This is accomplished by internally dividing the devices such that the circuitry associated with the A-side is electrically isolated from the B-side. This dual supply architecture permits the LVX translator family to interface 3V signals and 5V signals with zero static power dissipation.

In the case of the 74LVX4245 device the A-side is dedicated to 5V operation and $V_{\rm CCA}$ is specified for the range 4.5V–5.5V. The B-side is dedicated 3.3V and $V_{\rm CCB}$ is specified for the range 2.7V–3.6V. The LVXC3245 and LVXC4245 offer further enhanced interfacing in that the B-side is designed to operate over an extended range of I/O and supply levels. For these types $V_{\rm CCB}$ is permitted to be

set to any value between 2.7V and 5.5V. The I/O levels on the B-side will track or scale automatically according to the level set on $V_{\rm CCB}$. This B-side operation is completely independent of $V_{\rm CCA}$. The A-port and control input buffers are referenced to $V_{\rm CCA}$ and do not vary with $V_{\rm CCB}$. Refer to Figure 4. The configurable dual supply translating transceivers (LVXC) are designed to tolerate floating inputs on the B-port when $V_{\rm CCA}$ and the control signals are set to valid operating levels. The combination of on-the-fly interface flexibility together with "empty socket" tolerance is intended to benefit designers of PC card systems where expansion cards with different supply potentials must be accommodated.

LVX-Low Voltage CMOS Bus

Along with the advanced interfacing capabilities offered by the LVX dual supply translators, these products offer switching speeds equivalent to 5V FCT/FAST but with Quiet Series noise performance and 3.3V supply.

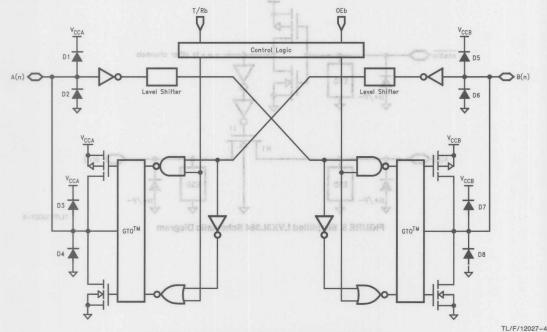


FIGURE 4. Simplified LVX Translator Schematic Diagram

LVX—Low Voltage CMOS Bus **Switches**

The LVX3L383 and LVX3L384 low impedance switches complete the LVX family. By virtue of their low "on" resistance these ten channel NMOS pass gates can be used to provide a high speed, bi-directional interface between mixed supply busses. Figure 5 depicts a single channel representation of the LVX3L384.

The enhancement type NMOS pass gate N1 utilized in all LVX3L383 and LVX3L384 low impedance switches provides bi-directional signal level translation capability. The source (Note 1) of the pass gate will always be clamped to Vg-Vtn irrespective of the drain potential. Vg is set by VCC via inverter I1. Consider the following case:

- V_{CC} is set to 4.1V Along with the advanced interfacing cap
- Vtn = 0.8V

- Vas= 5.0Vevisosers translating transcrive VOI = 15.0Vevisosers translating t
- Venable = 0V us beam and of dapproach to the mixed survey
- Vb is initially discharged

Given these conditions pass gate N1 saturates (Vds > Vgs Vt) and begins charging its source B(N) positively. As B(n) rises the difference between B(n) and V_{CC} (Vgs[N1]) decreases. When B(n) rises to within Vtn of VCC, N1 is cutoff and conduction ceases independent of the potential at A(n). The final terminal conditions then are

CMOS Translating Transceivers

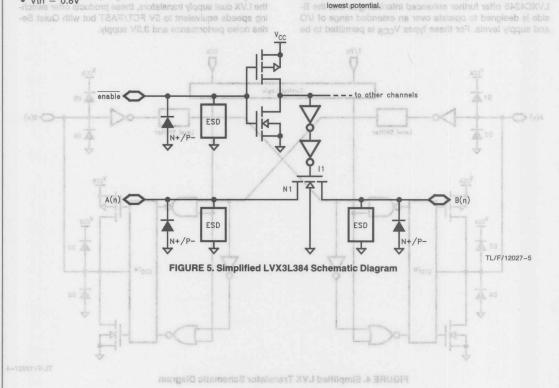
$$V[A(n)] = 5.0V$$

$$V[A(n)] = 5.0V$$

 $V[B(n)] = V_{OC} = Vtn = 3.3V$ be no including ve of be

and the translation is completed. I si shis-8 srt. V3.8-V3.A

Note 1: For an NMOS transistor the source is defined as the diffusion with LVXC4245 offer further enhanced inter stated as a Second residual Edition Edition in the Edition of the Edition Edition in the Edition Edition in the Editio



LCX—Low Voltage High Speed CMOS Logic (with 5V Tolerant Inputs and Outputs) agreed reflued According to the Country of the Cou

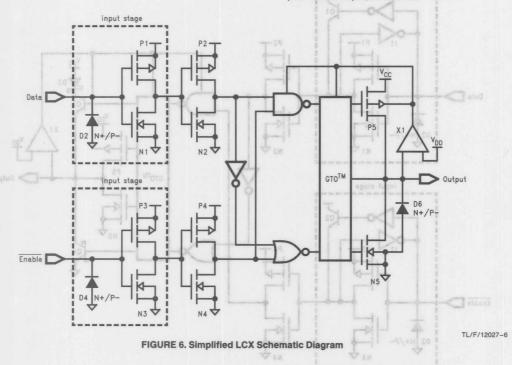
The LCX product line represents National Semiconductor's most advanced low voltage CMOS product line. These devices offer mixed 3V–5V capability and are recommended for applications where 3.3V and 5.0V subsystems interface with one another and where low power consumption is a necessity. By virtue of a proprietary input/output structure (Note 1), the LCX family of products will tolerate input and output (Note 2) node exposure to signals or DC levels that exceed the V_{CC} level. Refer to Figure 6 for schematic description of a typical LCX circuit.

LVT—Low Voltage High Speed BICMOS Logic

Note that the output PMOS device P5 has its bulk potential supplied by the output of the comparator X1 rather than by V_{CC} as in conventional CMOS. The circuitry contained within the comparator is designed such that the output is always the greater of V_{CC} or V_{O} . This technique circumvents the $P \pm /N -$ bulk-source forward junction that usually appears between the PMOS drain at the output and the bulk connection of the output PMOS which is usually tied to V_{CC} . Eliminating this junction is fundamental to the powered-down high Z and overvoltage tolerance features that distinguish LCX from other low voltage CMOS products.

Note 1: U.S. and international patent protection applied for.

Note 2: Output overvoltage is permitted unconditionally for tri-stated outputs. For active outputs, see datasheet.



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LVT—Low Voltage High Speed BiCMOS Logic

LVT is National Semiconductor's highest performance low voltage family of products. Manufactured using sub-micron BiCMOS technology, LVT includes all the mixed-supply interface features of LCX in addition to BJT-enhanced propagation delays. These 5V tolerant low voltage devices are recommended for applications where 3.3V and 5.0V subsystems interface with one another and where high speed and high drive are required. By virtue of hysteresis applied by I1 and I2 directly at the input node (refer to Figure 7), LVT devices will tolerate floating input conditions that would otherwise lead to increased leakage or compromises in system data integrity.

The output buffer design is based upon the LCX circuit and includes overvoltage tolerance at the output as does LCX. AC and DC performance in the LVT version of the output is augmented by the addition of the parallel NPN devices Q3 and Q4. The Q4 base drive required to sink the rated $l_{\rm OL}$ results in a nominal $l_{\rm CCL}$ of less than 10 mA. The reverse-biased Schottky device D3 prevents output overvoltages that exceed BVCEO from corrupting the low voltage supply. LVT benefits from this protection when $V_{\rm CC}$ is applied as well as when the device is powered-down.

LCX-Low Voltage High Speed CMOS Logic (with 5V Tolerant

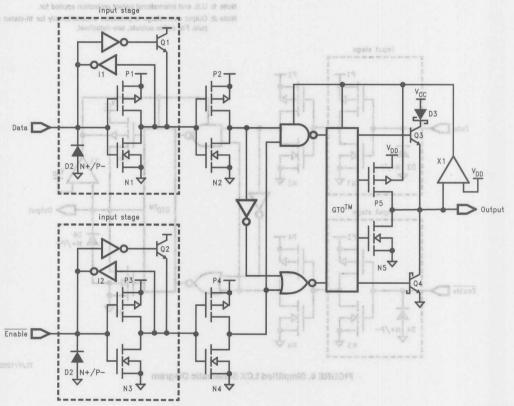


FIGURE 7. Simplified LVT Schematic Diagram

TL/F/12027-7

At National Semiconductor it is our mission to excel in serving chosen markets by delivering semiconductor intensive products and services of the highest quality and value, thereby providing a competitive advantage to our customers worldwide. Should you have any additional questions about our Low Voltage Products, please contact your local sales office or our Customer Response Center at 1-800-272-9959 within the U.S., 1-800-258-6768 in Canada.



Section 2 Contents

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Low Voltage Logic Ratings, Specifications, and Waveforms

put and a voltage 0.3V below the state came state and a voltage of the local restaurance the

DC Characteristics	HIGH level to a high impedance (OFF) state.
Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.	V _{IH} Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level. V _{IHD} Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during
Voltages: All voltages are referenced to the ground pin. All voltage limits are specified as absolute values. ICC The current flowing into the V _{CC} supply terminal when the device is at a quiescent state.	a Multiple Output Switching (MOS) operation. VIL Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level. VII D Dynamic Input LOW Voltage. The maximum input
I _{CCH} The current flowing into the V _{CC} supply terminal when the outputs are in the HIGH state.	voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.
I _{CCL} The current flowing into the V _{CC} supply terminal when the outputs are in the LOW state.	VOH Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load
Additional I _{CC} due to TTL HIGH levels forced on CMOS inputs. I _{CCZ} The current flowing into the V _{CC} supply terminal when the outputs are disabled (high impedance).	and V _{CC} supply voltage. V _{OL} Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V _{CC} supply voltage.
I _I , I _{IN} Input Current. The current flowing into or out of an input when a specified LOW or HIGH voltage is applied to that input.	V _{OLP} Maximum (peak) voltage induced on a static LOW output during switching of other outputs. V _{OLV} Minimum (valley) voltage induced on a static
Output HIGH Current. The current flowing out of an output which is in the HIGH state.	LOW output during switching of other outputs. AC Characteristics
Output LOW Current. The current flowing into an output which is in the LOW state. Output Short Circuit Current, The current flowing	f _t Maximum Transistor Operating Frequency—The frequency at which the gain of the transistor has dropped by
out of an output in the HIGH state when that out-	three decibels. fmax Toggle Frequency/Operating Frequency—The
V _{tp} , L _{eff} , etc.) which have been shown to sig. (lsit arity affect	maximum rate at which clock pulses may be applied to a

tive setup time indicates that the correct logic level may be

maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

tpLH Propagation Delay Time-The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

tpHL Propagation Delay Time-The time between the specified reference points, on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

tw Pulse Width-The time between specified amplitude points of the leading and trailing edges of a pulse.

th Hold Time-The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

I_{I(HOLD)} Input hold Current. Input current that holds the

-ibnoo bn output.

input at the previous state when the driving device goes to a high impedance state.

Input over-drive current. Input current that is I(OD) specified to switch a logic level which is held at previous state. Is noisulmoo eouber of hotile ris mi

IOZ Output OFF current. The current flowing into or

out of a disabled TRI-STATE® output when a

specified LOW or HIGH voltage is applied to that

IOFF Input/Output power-off leakage current. The maximum leakage current into or out of the input/ output transistors when forcing the input/output from OV to 5.5V with V_{CC} = OV. beginning ad

Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

VJK Input Clamp Diode Voltage. The voltage on an input (-) when a specified current is pulled from that input.

ts Setup Time—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

tpHZ Output Disable Time (of a TRI-STATE Output) from HIGH Level—The time between specified levels on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

tpLZ Output Disable Time (of a TRI-STATE Output) from LOW Level—The time between specified levels on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

tpzH Output Enable Time (of a TRI-STATE Output) to a HIGH Level—The time between the specified levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

tpzL Output Enable Time (of a TRI-STATE Output) to a LOW Level—The time between the specified levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

trec Recovery Time—The time between the specified level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

Multiple (Simultaneous) Output Switching Propagation Delays—These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF output load.

Multiple Output Switching Skew—Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

AC Dynamic (Noise) wodA studio latinoupee Characteristics

V_{OLP}, V_{OLV}—Ground Bounce (Quiet Output Switching)—Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that V_{CC} and Ground move internal to the IC.

VILD, VIHD—Dynamic Threshold—Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

tion. A negative hold time indicates to level may be released prior to the acInput Edge Rate—This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

Power

Power-Up I_{CC} Traces—Shows how the supply current reacts to various input conditions during power up.

 I_{CC} vs V_{IN} Traces—Traces of I_{CC} vs V_{IN} show how the supply current changes with input voltage.

 I_{CCD} (Dynamic I_{CC})—Determines the amount of current an IC will consume at frequency.

Capacitance beniles at menus evilico9 :amenus

Input/Output Capacitance (C_{IN}/C_{OUT})

Power Dissipation Capacitance (C_{PD})

Reliability Tests noter or a regation IIA :segation

Latch-Up—Testing determines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

Electrostatic Discharge, Human Body—Per MIL-STD-883C and Machine model.

Characterization Philosophy

During the National new product introduction process for logic IC's, a new low voltage IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta, $V_{\rm tp}$, $V_{\rm tp}$, $L_{\rm eff}$, etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester, $V_{\rm CC}$, temperature, and condition. This allows product to be shipped on demand without problems or delays.

Power Dissipation—Test Philosophy of Signature of Desired

In an effort to reduce confusion about measuring power dissipation capacitance, CpD, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements,

Power Dissipation—Test

Philosophy (Continued)

the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation capacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

Gates/Buffers/ Line Drivers: Switch one input. Bias the remaining inputs such that one output switches.

Latches:

Switch the Enable and D inputs such that the latch toggles.

Flip-Flops:

Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-

Decoders: Switch one address pin which changes two outputs.

Multiplexers: Switch one

Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.

Counters: Switch the clock pin with other inputs biased such that the device counts.

Shift Registers: Switch the clock pin with other inputs bi-

ased such that the device shifts.

Transceivers: Switch one data input. For bidirectional

devices enable only one direction.

Parity Generator: Switch one input.

Priority Encoders: Switch the lowest priority input.

AC Loading and Waveforms

LOADING CIRCUIT

Figure 1 shows the AC test circuit used in characterizing and specifying propagation delays for all of the low voltage logic devices as shown, unless otherwise specified in the data sheet of a specific device.

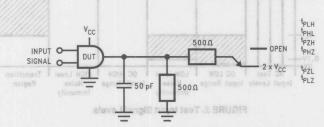


FIGURE 1a. AC Test Circuit for LVQ, LVX Translator Families

FIGURE 1b. AC Test Circuit for LVX Family

TEST SIGNAL DUT TO PEN TO THE TOTAL THE TO

Family	VI
LCX	6V
LVT	6V
LVX Bus SW	7V

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TL/F/12010-1

TL/F/12010-25

FIGURE 1c. AC Test Circuit for LCX, LVT, LVX Bus Switch Families

Test Conditions

Figure 2 describes the input signal voltage levels to be used when testing low voltage logic circuits. The AC test conditions follow industry convention requiring $V_{\rm IN}$ to range from 0V to $V_{\rm CC}$. The DC parameters are normally tested with $V_{\rm IN}$ at guaranteed input levels, that is $V_{\rm IH}$ to $V_{\rm IL}$ (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Priority Encoders: Switch the lowest priority input.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 3.3V then dropping it to a level corresponding to V_{IH} characteristics, and then raising it again to the 3.3V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0V to V_{IL} , then returning to 0V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A $V_{\rm CC}$ bypass capacitor should be provided at the test socket, also with minimum lead lengths.

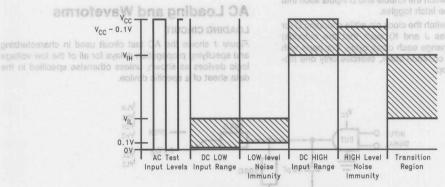


FIGURE 2. Test Input Signal Levels

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			Vec	
OPEN IPLH: IPHL	D		1	TURMI
	-0/-1	Andread Contraction	TUB	
	-0		windows.	
		15/50 pF		
		86.5		

FIGURE 1b. AC Test Circuit for LVX Family

Family
LCX

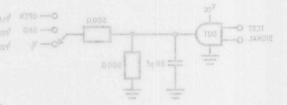


FIGURE to, AC Test Circuit for LCX, LVX, Bus Switch Families

Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc. See *Figures 3* and 4.

Enable and Disable Times

Figures 5 and 6 show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from V_{OL} or V_{OH} , respectively. This change enhances the repeatability of measurements, and gives the system

Waveforms

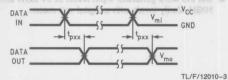


FIGURE 3. Waveform for Inverting and Non-Inverting Functions

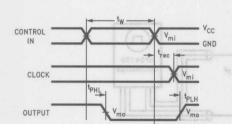


FIGURE 4. Propagation Delay, Pulse Width and t_{rec} Waveforms

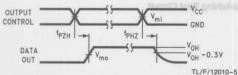


FIGURE 5. TRI-STATE Output High Enable and Disable Times for Low Voltage Logic

designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the 10% and 90% points. This better reflects actual test points and does not change specification limits.

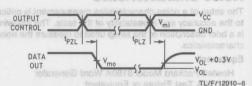


FIGURE 6. TRI-STATE Output Low Enable and Disable Times for Low Voltage Logic

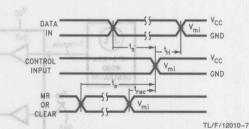


FIGURE 7. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

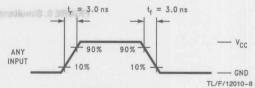


FIGURE 8. trise and tfall

V _{mi}	V _{mo}
50% V _{CC}	50% V _{CC}
50% V _{CC}	50% V _{CC}
50% V _{CC} *	50% V _{CC}
1.5V	1.5V
1.5V	1.5V
	50% V _{CC} 50% V _{CC} 50% V _{CC} * 1.5V

^{*1.5}V for TTL Compatible

TL/F/12010-4

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to low voltage logic devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all parts of the tester, which are near the device, are conductive and connected to ground.

Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics.

Equipment:

Hewlett Packard Model 8180A Word Generator PC-163A Test Fixture or Equivalent HP54100 Oscilloscope or Equivalent

Procedure:

- 1. Verify Test Fixture Loading: Standard Load 50 pF.
- 2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.

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- Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
- 4. Set V_{CC} to 3.3V. 1 easier tucture and energy thing and ta
- Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
- Set the word generator input levels at 0V LOW and 3.3V HIGH. Verify levels with a digital volt meter.

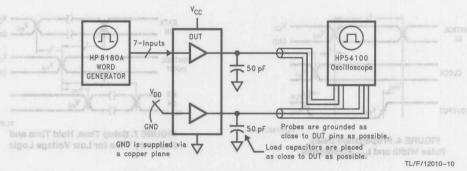


FIGURE 9. Simultaneous Switching Test Circuit

Noise Characteristics (Continued)

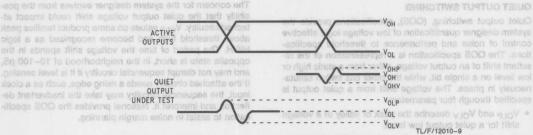


FIGURE 10. Quiet Output Noise Voltage Waveforms

Note 1: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 2: Input pulses have the following characteristics: f = 1 MHz, $t_f = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

VOLP/VOLV and VOHP/VOHV:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 10 k Ω scope probe plugged into a standard SMB type connector on the test fixture.
- Measure V_{OLP} and V_{OLV} on the quiet output LOW during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

VII D and VIHD:

- Monitor one of the switching outputs using a 10 k Ω scope probe plugged into a standard SMB type connector on the test fixture.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output low level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Extended Specifications

National has taken new steps in aiding the system designer with a better method to predict device performance in his application. National now offers system oriented performance specifications so a designer can feel confident in the way a device will perform over a wider variety of switching conditions. Performance specifications in the form of Extended Specifications are provided with each product datasheet.

In the past, most extended databook specifications depended on a representative product family function to provide the guaranteed performance data for the rest of the family. The drawback from this method of test and specmanship leaves rather large process, tester and function guardbands in the final maximum or minimum specifications. The test data for National's low voltage logic product family, taken during product development on each function, provides the low voltage logic family with device specific and guaranteed extended specifications that can be passed directly to the system designers. National offers the extended specifications with the belief that customers can reduce their incoming test requirements and in essence reduce the cost and time for product design-in.

Additional specifications provided by National include: Quiet Output Switching (QOS) V_{OLP} , V_{OLV} , and Dynamic Threshold (DVTH), V_{ILD} , and V_{IHD} .

Each of the guaranteed extended specifications involve multiple output switching events. During a multiple output switching event, stray inductance and capacitance inhibit product performance. National has developed standardized hardware that aligns with the industry for low voltage logic product evaluations. Some of the features of the test fixturing include ground planes and low inductive connections, critical in evaluating the product and not the fixture.

The extended specfication tests have very similiar if not identical test setups. The results of the measurements from each test depend on the application focus. The quantitative analysis from the tests provides insight into product performance. The parameters and typical results from each test type can be easily explained in the sections that follow.

TABLE I. Test Conditions for QOS, DVTH

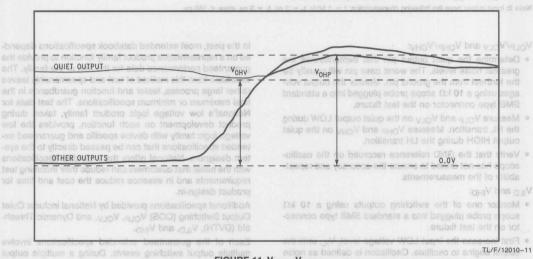
Parameter	Value
Input Edge Rate	2.5 ns
Input Skew	< 300 pS
Input Amplitude	0V to 3.0V
Input Frequency	1 MHz
Output Load	50 pF

QUIET OUTPUT SWITCHING

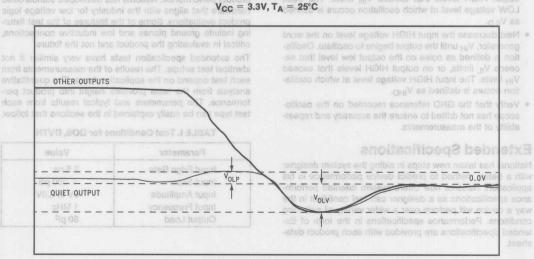
Quiet output switching, (QOS), specifications provide the system designer quantification of low voltage logic effective control of noise and performance to threshold specifications. The QOS specification is a representation of the resultant shift of an output voltage, either from a static high or low level on a single bit, while the other bits switch simutaneously in phase. The voltage shift from a quiet output is specified through four parameters.

- V_{OLP} and V_{OLV} describe the peak or valley of a voltage shift for a quiet output low level.
- V_{OHP} and V_{OHV} describe the peak or valley of a voltage shift for a guiet output high level.

The concern for the system designer evolves from the possibility that the quiet output voltage shift could impact attached circuitry. V_{OLP} values on some product families peak above threshold high and become recognized as a logic HIGH. The period of time the voltage shift spends in the opposite state is short, in the neighborhood of 10–100 pS, and may not disrupt sequencial circuitry if it is level sensing. If the attached circuitry needs a rising edge, such as a clock input, the sequencial circuitry may take the inadvertent deflection and interpret it. National provides the QOS specification to assist in noise margin planning.



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FIGURE 12. V_{OLP}, V_{OLV} HL Transition V_{CC} = 3.3V, T_A = 25°C

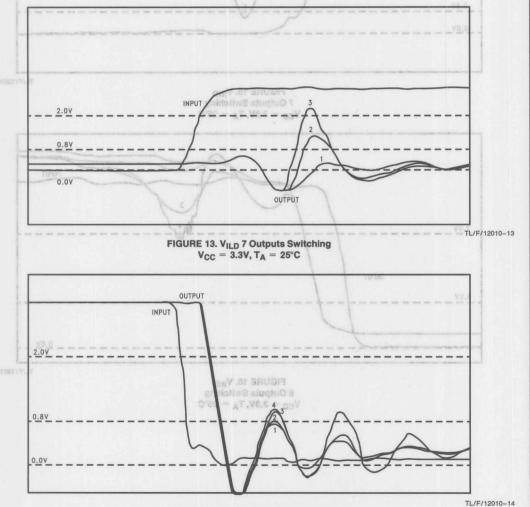
Dynamic threshold data, (DVTH), like QOS data, provides the system designer with noise performance criteria. DVTH specifications quantify the magnitude of output voltage deflection that a logic high or low might experience under a multiple output switching condition. The voltage deflection is a result of an apparent shift of an input's threshold due to noise generated from MOS switching on the internal die ground and V_{CC} busses. The phenomenon occurs during any logic state transition: LH, HL, ZL, etc. As a practice, National determines the worse case transition for each product and generates the specification based on that tran-

Dynamic threshold specifications are denoted by the nomenclature, VII D and VIHD, where the "D" represents "Dynamic". The definitions for each are as follows,

- DYNAMIC THRESHOLD in softe V0.5 to level floid blodesoft turns . VILD The maximum LOW input level such that normal switching/functional characteristics are observed on the
 - V_{IHD} The minimum HIGH input level such that normal switching/functional characteristics are observed on the

Dynamic threshold failures are bundled into five main failure modes. The most predominant failure is an output deflection in violation of an input threshold level. Others include propagation delay step out in excess of an MOS propagation delay specification, state changes and oscillations. A detailed definition of each failure can be described as follows,

On a low output, the LOW level will not rise above an input threshold low level of 0.8V after the transition of the output. Figures 13 and 14. Numbered output curve deflections are a result of 10 mV incremental changes on the low input signal level.



2. On a high output, the HIGH level will not drop below an input threshold high level of 2.0V after the transition of the output. Figures 15 and 16. Numbered output curve deflections are a result of 10 mV incremental changes on the high input signal level.

Extended Specifications (Continued)

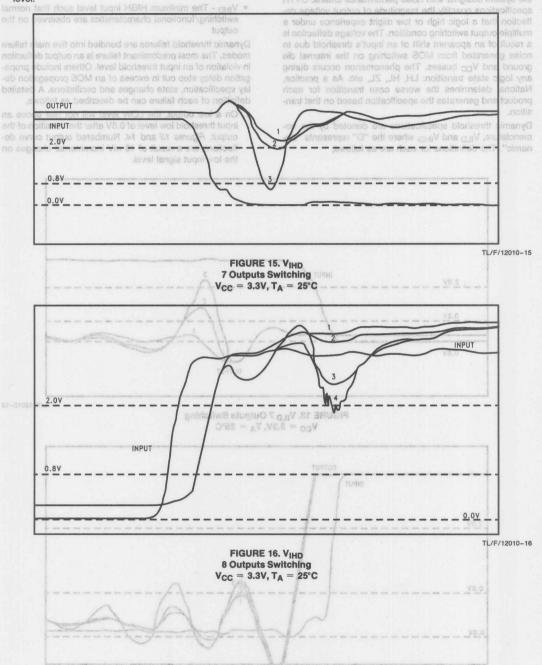
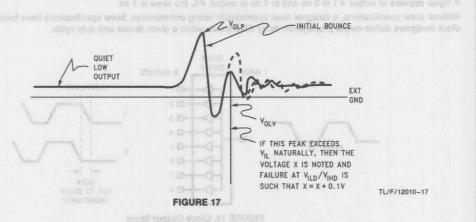


FIGURE 14. VILD 8 Outputs Switching

- 3. If the natural ringing, other than the initial bounce, of the output violates an input threshold level, the starting voltage level is noted and monitored until a 100 mV amplitute change towards threshold. If no amplitude change occurs, then the next peak or valley on the output is monitored for input threshold violation. Figure 17.
- The propagation delay is monitored and is determined a failure when it exceeds the MOS propagation delay for that transition.
- Gross failures including oscillation and functional state changes.



Total system clock skew includes intrinsic sitew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic sitew is defined as the differences in tace delays and loading conditions.

| INTERNSIC SICE | EXTRINSIC SICE | OUT | CLOCK OUT | CLO

Mila signals produces 20 ns clock cycles

stal system skew budget = 10% of clock cycle* = 2 ns → 2 ns

If extinsic skew = 1 ns → −1 ns

Device skew (Intinsic skew) must be less than 1 nst ← 1 ns

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into low Voltage devices. This section provides general definitions and examples of skew.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See Figure 18, stressed separate et al.

Example

If signal appears at output #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device and duty cycle.

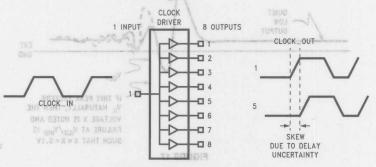


FIGURE 18. Clock Output Skew

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Extended Specifications (Continued)

age level is noted and monitored until a 100 mV ampli-

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

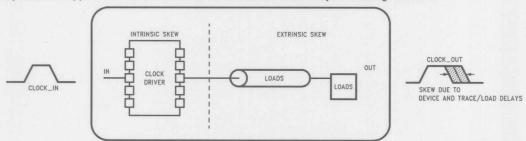


FIGURE 19. Sources of Clock Skew

Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles

Total system skew budget = 10% of clock cycle* = 2 ns → 2 ns

If extrinsic skew = 1 ns → -1 ns

Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design Rule of thumb.

2

Skew Definitions and Examples (Continued)

CLOCK DUTY CYCLE

• Clock Duty Cycle is a measure of the amount of time a signal is HIGH or LOW in a given clock cycle.



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Duty Cycle = t/T * 100%

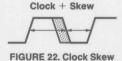
FIGURE 20. Duty Cycle Calculation



тHI

FIGURE 21. Clock Cycle

· Clock skew effects the Duty Cycle of a signal.



Example:

 $t_{\mbox{\scriptsize HIGH}}$ and $t_{\mbox{\scriptsize LOW}}$ are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE II

System Frequency	Skew	tHIGH	tLOW			Duty Cycle
50 MHz 50 MHz 50 MHz	0 ns 2 ns 1 ns	10 ns 12 ns 11 ns	10 ns 8 ns 9 ns	50/50% 60/40% 55/45%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen a higher frequencies.

Definition of Parameters

tosly, tosyl (Common Edge Skew)

toshl and toshl are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, toshl collections to be minimized.

Definition

toshl, toslh (Output Skew for High-to-Low Transitions):

toshl = |tphlmax - tphlmin|

Output Skew for Low-to-High Transitions:

toslh = |tplhmax - tplhmin|

Propagation delays are measured across the outputs of any given device.

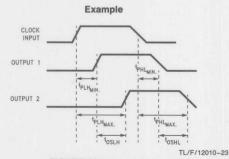


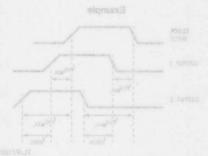
FIGURE 23. toslh, toshl







Duty Cycle			нынд	Skeyr	Syntem Frequency
	50/50% 60/40% 55/46%	en 01 en 8 en e			50 MHz 50 MHz 50 MHz
Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.					





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Quality and Reliability
ntroduction
Qualification Requirements for Logic Integrated Circuits
Quality Information and Communication (QUIC) System
Vafer Level Reliability (WLR)
Electrostatic Discharge (ESD) Sensitivity
Repeatability of Human Body Model (HBM) ESD Results
Power Sensitivities for Minimum Geometry Products
Section 2 Testing

Quality and Reliability

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Quality and Reliability



(OASD) maintains a variety of data trace trace. While as: Electronic Reliability beta Managem **Villidability and Reliability** Peta Managem **Villidability and Reliability** Burn-in Board Inventory, and a number of specific process of "good" devices to an unacceptable

Introduction solved A still metays belonger and

Product qualification is a disciplined, team activity which focuses on demonstrating, through the acquisition and analysis of engineering data, that a device design, fab process, or package design meets or exceeds minimum standards of performance. In most cases, this involves running samples of product through a series of tests which expose the samples to operating stresses far in excess of those which would be encountered in even the most severe "real life" operating environment. These tests are called either accelerated stress tests or accelerated life tests. A properly designed qualification test sequence exposes, within a matter of days or weeks, those design, materials, or workmanship defects which would lead to device failure in the customer's application after months or even years of operation.

In order to be considered a "world class" supplier of semiconductor devices, NSC designs and manufactures products which are capable of meeting the reliability expectations of its most demanding customers. While customer requirements and expectations vary on the subject of reliability requirements for devices, virtually all large users have general procurement specifications which establish failure rate goals or objectives for the suppliers of the components used in their products.

Failure rate goals for infant mortality and long-term-failure-rate-in-service have been established for all NSC product lines. These goals are published internally at the beginning of each fiscal half-year (usually June and December). The actual performance of the product against these goals is measured monthly using life test data gathered from various sources including the Fast Reaction and Long Term Audit Program. Performance is reviewed every six (6) months by Reliability and Product Group management and adjusted as necessary to reflect customer expectations, competitive data, and/or historical performance trends.

Given that product reliability is an overriding corporate objective, and that any deficiency in design, materials, procedures, or workmanship, has a potential for adversely affecting the reliability of the product, Manufacturing and Engineering organizations within NSC, its subsidiaries, and its sub-contractors, involved in introducing a new device, process, or package, share a joint responsibility for demonstrating that the product does conform to NSC standards and to the standards and expectations of NSC's customers.

As a matter of policy, it is NSC's goal to design and manufacture product that is 100% defect-free and capable of surviving the qualification tests with zero failures. This policy is not interpreted as a directive to abandon a qualification pro-

gram when failures occur or to delay new product releases until perfection has been achieved. Rather, the policy is intended to focus engineering resources on the identification and elimination of the design, process, or workmanship deficiencies that are the root causes of the failures and then to engineer a solution to correct those deficiencies.

Specific family qualification data is available and may be obtained by calling our customer response center at 1-800-272-9959 within the US. 1-800-258-6768 in Canada.

Qualification Requirements for of short Control of the Logic Integrated Circuits

st 12 test mony or 2400, 4800 o	Test Method	Test/Stress Conditions	Sample Size Each Lot
Operating Life	SOP-5-049-RA Method 107	1000 Hours @T _A = 125°C	77
High Tempera- ture Storage	SOP-5-049-RA Method 103	1000 Hours @150°C	45
Temperature Cycle	SOP-5-049-RA Method 105	1000 Cycles -65°C to +150°C	773
Temperature Cycle with Preconditioning	SOP-5-049-RA Method 105	1000 Cycles -65°C to +150°C	(lithabl 8
Temperature- Humidity-Bias	SOP-5-049-RA Method 104	1000 Hours 85°C @ 85%RH	77
Temperature- Humidity-Bias with Precon- ditioning	Method 112 Method 104	Precondition plus 100 hours 85°C to 85%RH	4. Nation 77 nbe active custom
Autoclave day	Method 101	500 hours 121°C @ 15 psig	45
Thermal Shock	Method 106	100 Cycles -65°C to +150°C	22
Salt Atmosphere	Method 209	25 Hours 35°C	22
Resistance to Solvents	Method 207	4 Solvents	3 Each Solvent
Lead Integrity	Method 205	Condition as Appropriate to Package	22 Leads
Solderability	Method 203	8 Hour Steam 5 secs @260°C	22
Solder Heat	Method 204	12 secs 260°C	22

Quality Information and Communication (QUIC) System

BACKGROUND

National's Quality Assurance Systems Development group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Failure Analysis (F/A), Burn-in Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is programmed to recognize each individual user of the system at the point of logging on to the mainframe, and provides an appropriate list of menu options consistent with the user's level of access requirements.

National grants access to QUIC by customers that provides a sufficient level of security over the entire system, thus precluding the possibility of accidental access (or even damage) to various files.

HOW A CUSTOMER LINKS TO QUIC

 Check to make sure you have the hardware components listed below. (An attached printer is desirable but not imperative.)

IBM/PC compatible computer with at least 128k memory. Hayes compatible 1200 baud modem (or 2400, 4800 or 9600).

Touch tone phone. To to bordeM

- Request access to QUIC by contacting your National sales representative or Customer Service Center at 1-800-272-9959, who will coordinate all activities necessary to provide access for your company and arrange training (usually handled over the telephone).
- Identify the person who will be your company's main contact and user of the QUIC system. This person will assume responsibility for the USERID assigned to your company and will receive training on how to access and use the QUIC system.
- 4. National will provide a USERID, password and account number with appropriate menus and a communications software package called EXECULINK, which allows the customer's PC to talk with NSC's host computer and also turns the PC into a virtual host terminal, with full-screen editing capability and full use of program function (PF) keys. EXECULINK also provides for file transferring between host and PC and spooling of print files to a PC-attached printer.

ONGOING IMPROVEMENTS

As we receive feedback from the users of QUIC, we (QASD) will continue to enhance the "User Friendliness" of the system and add new features which, we hope, will help promote a true sense of teamwork between us and our customers.

Wafer Level Reliability (WLR)

BACKGROUND

The conventional methods of reliability screening, that of short-term burn-in to eliminate infant mortalities and long-term life tests at high temperature, will soon become impractical for many devices. The reasons for this are tighter infant mortality ppm requirements, higher costs, and shortened lifetimes.

As device complexity increases, the testing sample size required to ensure infant mortality ppm levels in the 0–10 ppm range will quickly deplete reliability test capacity. While burn-in eliminates inferior devices, it can also substantially shorten the lifetimes of "good" devices to an unacceptable level, creating an expensive and somewhat risky procedure. New technology advances which minimize geometry, have moved our device lifetime distributions closer to our customer's expected system life. As device geometries shrink, resulting in higher current densities, electric fields, and chip temperatures, tighter fab process control and instant feedback become critical.

THE GOAL OF WAFER-LEVEL-RELIABILITY TESTING-PROCESS RELIABILITY

Wafer-level-reliability testing represents a proactive, correlation and control approach to ensuring device reliability. WLR is not meant to replace classical reliability testing. Instead it is used to supplement existing methods.

WLR testing is used to: sometimes feet not softlicuo bemple

- 1. Identify shifts in On-Line Process Controls (fab monitors) which affect product reliability.
 - 2. Reduce process qualification cycle time.
 - 3. Improve process qualification success rate.
 - 4. Assess reliability trends of production processes.
 - 5. Quantify the reliability impact of process modifications.

WLR provides faster feedback for fab process control. The collection of WLR test data during and at the end of wafer fab processing provide a reliability baseline for each of our fab processes. Shifts in WLR test results, whether intentional (a process change or qualification) or unintentional (a process control problem), signal an increase or decrease in product reliability risk. WLR monitoring of production processes using Statistical Quality Control (SQC) techniques provides engineering with the information required to find and fix process control problems faster, and to determine the effectiveness of on-line process controls from a reliability standpoint. In this way, WLR testing is used to link on-line process controls to the traditional accelerated life testing methods.

NATIONAL'S WLR PROGRAM

National developed a corporate-wide WLR program which continues to implement powerful, new test techniques. WLR testing has been used effectively to help understand how process variability affects product reliability. It is also used to help build-in reliability at the design stage for new process technologies such as those used by the Low Voltage logic families.

WLR tests and test structures have been designed to increase the likelihood and predict a rate of a reliability failure mechanism occurrence. In addition, National has developed a partnership with a leading parametric test system supplier. Working together, a WLR test system was designed and developed to meet the unique requirements of Wafer-Level-Reliability testing. These systems are capable of testing to the voltage, current, and temperature extremes required for inducing the desired failure mechanisms in a short period of time. Some examples of the reliability failure mechanisms that are monitored using WLR techniques include:

Wafer Level Reliability (WLR) (Continued)

Interlayer Dielectric Integrity

Unique high voltage testing (to 1500V) is used to test for dielectric particles, metal hillocks or contamination, and poor dielectric stop coverage. Designed experiments have been successful in correlating the high voltage WLR test results to fab process monitors (such as deposition temperature and etch selectivity), and to accelerated life test results (Op-life, Temp Cycle, and Thermal Shock).

Metal Step Coverage

High current testing of large area metal serpentine structures is performed to detect restrictions in the conducting stripe. Designed experiments have been successful in correlating the high current WLR test results to fab process monitors such as metal thickness, critical dimensions, and via size.

Mobile Ions

A 200°C hot chuck is used with custom-built high temperature probe cards to accurately measure transistor threshold voltage shifts for a variety of oxide layers. Other methods for detecting mobile ion contamination include the use of self-heated polysilicon gate test structures and Triangular Voltage Sweep (TVS) test techniques.

Metal Stress Voids alvab easilg of endifibring O'll guiled .s.

High current resistance measurements are taken before and after wafers are processed through a series of heating and cooling cycles. This heat treatment is designed to mimic the high temperature processing incurred during device assembly (such as a seal-dip furnace), and it has been shown to accelerate metal void formation when the stress of the overlying film is high enough. Significant increases in the final resistance indicate the formation of metal stress voids.

Gate Oxide Integrity:

JEDEC J_{RAMP}, V_{RAMP} and Q_{BD} test techniques are used to monitor gate oxide quality. The WLR tester is also used to perform very sensitive leakage current measurements, using a specially designed picoammeter module, which allows us to detect subtle differences in gate oxide quality.

Passivation Integrity on bus hebracelle ad bluoris guillest

A novel wafer-level-autoclave test technique has been developed which allows us to quantify the level of protection the passivation film provides when the wafer is subjected to a high temperature, high humidity environment.

Hot Electron Degradation

Two wafer level tests are performed to indicate device susceptibility to hot electron damage. First, the maximum substrate current is measured to indicate the level of impact ionization occurring at the drain edge. Second, gate current measurements are taken to gauge the magnitude of electron injection during device operation. Long-term DC stressing of transistors at peak substrate current conditions is also monitored.

Electromigration

A Standard Wafer Electromigration Accelerated Test (SWEAT) technique is used to measure the sensitivity of a metal line to electromigration failures. SWEAT is used as a relative test of the reliability of a line.

Contact Electromigration

Risk of failures due to contact spiking and solid phase epitaxial growth (SPEG) are monitored by forcing current through specially designed test structures, and monitoring increases in resistance and substrate leakage.

Repeatability of HBM ESD Results

Electrostatic Discharge Sensitivity (ESD)

Low Voltage logic products are manufactured using either submicron CMOS or BiCMOS technology. To protect these circuits from the harmful effects of Human Body Model (HBM) ESD events, proprietary protection circuitry along with traditional ESD diodes are used.

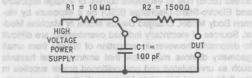
By design, this circuitry improves immunity to both HBM and Electrical Overstress (EOS). Protection from pin-to-ground (GND), pin-to- $V_{\rm CC}$ is achieved through traditional diodes. Additional protection is provided via proprietary solutions that provide a low resistance path between $V_{\rm CC}$ and GND during various ESD zap combinations.

The device design and layout ensures dependable turn-on characteristics as well as robustness.

ESD protection was achieved with no appreciable affect on speed or increase in capacitance.

Low voltage logic ESD sensitivity is guaranteed greater than 2000V, using the MIL-STD-883C, test method 3015 for Human Body Model (HBM) ESD.

HBM Test Circuit



TL/F/11564-2

Normal handling precautions should be observed as in the case of any semiconductor.

Repeatability of HBM ESD Results

Research has shown that stray capacitance in the ESD testers can cause device degradation or early ESD failure. For this discussion, stray capacitance is defined as capacitance that is distributed from the device socket through the board connections and lines to the HBM R-C network: $1500\Omega\pm1\%$, and charging capacitor: $100~\mathrm{pF}\pm10\%$. This degradation is seen mainly in N-channel protection and is caused by the charge delivered by the stray capacitance, charge that is not accounted for in MIL STD-883C/3015.7.

Lowering stray capacitance in the tester is advocated by the EOS/ESD Association under their EOS/ESD-S5.1-1991 spec. This specification helps to improve tester-to-tester repeatability independent of part type, by designating ESD zap waveform guidelines, similar in fashion to those of MIL STD-883C/3015.7. The waveform guidelines ensure that stray capacitance of the tester will be limited to 30 pF or less

The EOS/ESD Association has recommended EOS/ESD-S5.1-1991 be used in conjunction with MIL STD-883C/3015.7 to provide a better testing environment as well as the most representative HBM ESD zap waveform. Using this methodology will provide greater repeatability without compromising the intent of HBM ESD testing.

Repeatability of HBM ESD Results

(Continued)

More information on stray capacitance and the EOS/ESD S5.1-1991 can be found in the 1993 EOS/ESD Symposium Proceedings' article "Analysis of HBM ESD testers and specifications using a 4th order lumped element model", pp. 129–137.

Power Sensitivities for Minimum Geometry Products

The demand for high performance process technology capable of faster speeds, minimal noise and lower operating voltages drives the microelectronics industry towards decreasing layout geometries. Advanced process technology minimizes gate widths, gate oxide thickness and junction depths to improve gate switching speeds. In contrast, the decreased geometries reduce the ability of the devices built on advanced processes to resist electrical overstresses. As geometries decrease, emphasis shifts towards the reduction of environmentally induced electrical overstresses to ensure system and component reliability.

Market trends continue to drive the need for smaller geometries with reduced power supply voltages. Current 5.0V technologies are migrating towards 3.0V technologies while 3.0V technologies have shown a greater sensitivity to electrical overstresses. Sensitivities to electrical overstresses have been observed in as large as 1.0 µm geometries.

Device damage from electrical overstresses vary and the categories include, but are not limited to: Electrical-Over-Stress (EOS) due to excessive current or voltage exposure and Electro-Static-Discharge (ESD) be it exposure by Human Body Model, Charged Device Model or Machine Model. Sources of electrically induced overstresses are difficult to determine; however, investigation of failures from small geometry devices may show that environmental hazards such as unregulated and unconditioned power supplies in the field exceed "Absolute Maximum Ratings" causing unrecoverable device damage.

In an effort to resolve device sensitivities to electrical overstresses, designers and engineers can reference device databooks. Databook specifications include "Absolute Maximum Ratings" and adherence to this specification is essential in ensuring component and system level reliability.

 A. Amerasekera, A. Chatterjee, "An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies", EOS/ESD Symposium, p5B.6.1.

±1%, and charging capaciton 100 pF ±10%. This decra-

Lowering stray capacitance in the tester is advocated by the EOS/ESD Association under their EOS/ESD-S5.1-1991 spec. This specification helps to improve tester-to-tester re-

3015.7 to provide a better testing environment as well as

Latchup Testing delies level retell

Latchup in CMOS and BiCMOS circuits can vary in severity from being a temporary condition of excessive I_{CC} current and functional failure, to total destruction requiring a new unit. The latchup condition is usually caused by applying a stimulus that is able to cause a regenerative condition in a PNP-NPN structure. For a more detailed description of definitions and causes of latchup, see National Semiconductor Application Note 600 (located in the "FACT Advanced CMOS Logic Data book" Lit. # 40019).

National has characterized its Low Voltage logic for robustness using an IMCS 4600 Automated Latchup Test System, complying to the JEDEC Standard No. 17. The automated test equipment approach to latchup provides a repeatable test setup and application of test conditions, reduces the amount of time for evaluation, and provides a more comprehensive set of vectors and stimuli over a shorter period of

The JEDEC Standard No. 17 is a standard measurement procedure for the characterization of CMOS integrated circuit latchup susceptability/immunity, measured under static conditions. The method allows for overcurrent/overvoltage stressing of inputs and outputs to detect latchup.

In short, the JEDEC Standard No. 17 follows a sequence of:

- 1. Apply power
- 2. Setup I/O conditions to place device in desired state
- 3. Apply trigger source for desired duration
- 4. Measure supply current appeared and professional base
- 5. Remove power supply if I_{CC} ≥ test limit loop bas and
- 6. Inspect for electrical damage

For Low Voltage logic products, all logic states are checked for a susceptibility to latchup with all outputs high, all outputs low, and all outputs in TRI-STATE®. If the device is a bi-directional device, then the logic states are tested in each direction. All inputs and outputs are tested for each logic state and direction.

For products with clamp diodes at inputs and outputs, a Positive and a Negative Current Trigger are required as stimuli for latchup. National characterizes latchup testing on all low voltage logic products at 125°C and at maximum supply voltage.

Due to the high trigger stresses, devices used for latchup testing should be discarded and not used for design, production, or other tests. Latchup testing is potentially destructive and may limit the life of a device.

tion the passivation tilm provides when the water is sub-

ectromigration

A Standard Wafer Electromigration Accelerated Test
(SWEAT) technique is used to measure the sensitivity of
a metal line to electromigration failures. SWEAT is used
as a relative test of the reliability of a line.



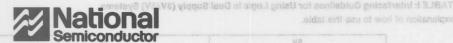
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Low Voltage Logic Applications and Design Considerations

Interfacing 3V/5V Logic

Introduction

Today's portable and battery-operated system designer is faced with the problem of keeping ahead when addressing system performance, long battery life and reliability. National Semiconductor's advanced CMOS Logic helps designers achieve these goals. Low Voltage CMOS Logic, like LVQ, LVX and LCX, are designed to alleviate many of the drawbacks that are common on present technology logic circuits. LV logic combines the low static power consumption and the high noise margins of CMOS with a high fanout, low input loading and at least 75Ω transmission line drive capability. Performance features such as advanced Schottky speeds at CMOS power levels, excellent noise suppression, ESD protection, and latch-up immunity are characteristics that designers of state-of-the-art systems re-

To fully utilize the advantages provided by LV logic, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common interfacing concerns relative to the performance and requirements of LV logic.

Table of Contents

- 1.0 INTERFACING DUAL VOLTAGE SYSTEMS
- 2.0 INTERFACING TO PURE 3V LVQ LOGIC
- 3.0 INTERFACING TO 5V TOLERANT LVX AND LCX
- 4.0 USING LVX3L383 AND LVX3L384 "ZERO DELAY" 10-BIT CMOS BUS SWITCHES FOR 5V TO 3V SIGNAL CONVERSION
- 5.0 USING LVX DUAL SUPPLY TRANSLATING LOGIC

Vow of the 74LVX4245 is greater than the Vin specification of the 74AC245 input and the Vot of the 74LVX4245 is less than

6.0 SUMMARY

1.0 Interfacing Dual Voltage Systems

In order to reliably interface one integrated circuit to another, recommended input and output specifications for voltage and current must be satisfied. Output specifications of the driving IC must meet the input requirements (VII and VIH) of the receiver IC in order for the circuit design to function properly. This "noise margin" protects the design against malfunction during system and environmentally generated

For better than two decades, almost all digital signal processing has been designed around a 5V standard power supply. During this period of time countless IC vendors have introduced new product families with higher drive, faster speeds, and lower power. As a result several Input/Output standards exist in the 5V world and interfacing between them can get confusing. Because of the inherent restrictions, pure-TTL technologies cannot operate with a 3.3V power supply. Therefore, the core technology for all 3V ICs will be MOS. In a straight 3V MOS system, all connections can be done directly, both on the outputs and on the inputs.

However, it will be quite some time before ALL components in a portable/desktop PC can operate at 3.3V. This is especially true for peripheral devices such as displays, printers, and faxes. Therefore, at some point in the system, 3V ICs must interface with 5V ICs. If mishandled, this interface will waste power and compromise reliability. On the following pages, solutions to possible dual voltage interfaces are out-Example: Suppose a 5V CMOS (i.e. 74AC245) ir.benile driven by a 3V/5V Translator (i.e. 74LVX3245) 3V o DIDOJ

TABLE I: Interfacing Guidelines for Using Logic in Dual Supply (3V/5V) Systems.

See example for an explanation of how to use this table.

			5V		3V			
	200	TTL 74F245	CMOS 74AC245	3V/5V Translator 74LVX4245	Pure 3V 74LVQ245	5V Tolerant 74LVX245	5V Tolerant 74LCX245	3V/5V Translator 74LVX3245
	a	V _{IH} = 2 V _{IL} = 0.8	V _{IH} = 3.85 V _{IL} = 1.35	V _{IH} = 2 V _{IL} = 0.8	V _{IH} = 2.4 V _{IL} = 0.8	$V_{IH} = 2$ $V_{IL} = 0.8$	V _{IH} = 2 V _{IL} = 0.8	$V_{IH} = 2$ $V_{IL} = 0.8$
	TTL 74F245 $V_{OH} = \text{(Note 1)} \\ V_{OL} = \text{(Note 1)}$	Yes Direct 0.7 0.25	No None -1.15 0.8	Yes Direct 0.7 0.25	OK (Note 2) 0.3 0.25	OK (Note 2) 0.7 0.25	Yes Direct 0.7 0.25	Yes Direct 0.7 0.25
5V	CMOS 74AC245 V _{OH} = (Note 1) V _{OL} = (Note 1)	Yes Direct 2,3 0.7	Yes Direct 0.45 1.25	Yes Direct 2.3 0.7	No None 1.9 0.7	Yes Direct 2.3 0.7	Yes Direct 2.3 0.7	Yes Direct 2.3 0.7
-/it	3V/5V Translator 74LVX4245 V _{OH} = (Note 1)	Yes Direct	No None -0.95	Yes Direct 0.9	Yes Direct 0.5	Yes Direct 0.9	Yes Direct 0.9	Yes Direct 0.9
no ten ber	V _{OL} = (Note 1) Pure 3V 74LVQ245 V _{OH} = (Note 1) V _{OL} = (Note 1)	O.7 OK Pull-Down 0.8 0.7	No None -1.05	O.7 Yes Direct 0,8 0.7	0.7 Yes Direct 0.4 0.7	0.7 Yes Direct 0.8 0.7	0.7 Yes Direct 0.8 0.7	Yes Direct 0.8 0.7
-01 18V	5V Tolerant 74LVX245 V _{OH} = (Note 1) V _{OL} = (Note 1)	OK TRI-STATE Outputs 0.8 0.7	No None -1.05 1.25	Yes Direct 0.8 0.7	Yes Direct 0.4 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7
test tuc ne ot	5V Tolerant 74LCX245 V _{OH} = (Note 1) V _{OL} = (Note 1)	OK TRI-STATE Outputs 0.8 0.7	No None -1.05 1.25	Yes Direct 0.8 0.7	Direct 0.4 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7	Yes Direct 0.8 0.7
3V Cs ons	Translator 74LVX3245	Yes Direct	Yes Direct	Yes Direct	Yes Direct	Yes Direct	Yes Direct	Yes Direct
its.	V _{OH} = (Note 1) V _{OL} = (Note 1)	0.7	0.55	0.7	0.7	0.7	0.7	0.7

Note 1: Refer to individual device datasheets for V_{OH} and V_{OL} levels. V_{OH} and V_{OL} are dependant on I_{OH} and I_{OL} values.

Typical values of V_{OH}/V_{OL} used to calculate noise margins.

1.0 INTERFACING DUAL VOLTAGE SYSTEMS Note 2: Regulate both 3V and 5V power supplies together to maintain a safe 5V V_{OH} to 3V V_{CC} delta. must interface with 5V ICs. If mishandled, this interface will 2.0 INTERFACING TO PURE BY LVG LOGIC

Example: Suppose a 5V CMOS (i.e. 74AC245) input is driven by a 3V/5V Translator (i.e. 74LVX3245) 3V outputs.

Receiver (Input)

		5V	10-BIT CMOS BUS SWASCHES FOR SV TO 3V		
	Driver (Output)	CMOS 74AC245	SIGHAL CONVERSION		
		V _{IL} = 1.35 V _{IH} = 3.85	.o using i.vx dual supply translating logic .b summary		
5V			According to Table I a 5V CMOS device, like the 74AC245, can be interfaced with a 3V/5V Translator, like the 74LVX4245, by directly connecting the input and output. This works because the V _{OH} of the 74LVX4245 is greater than the V _{IH} specification of the 74AC245 input and the V _{OL} of the 74LVX4245 is less than the V _{IL} specification of the 74AC245 input. Therefore a low or a high which ever is the case is maintained between the output to the input.		
3V	3V/5V Translator 74LVX3245 V _{OH} = (Note 1) V _{OI} = (Note 1)	Direct ← F 0.55 ← N	ov Volto interface? tecommended method loise Margin Low (V) = V _{IL} -V _{OL} loise Margin High (V) = V _{OH} -V _{IH}		

2.0 Interfacing to Pure 3V LVQ Logic

2.1 INTERFACING 5.0V TTL OR "REDUCED SWING" CMOS TO PURE 3V LVQ LOGIC

Bipolar TTL ICs or the newly introduced "reduced swing" (NMOS pull-up) CMOS ICs are the easiest of the 5V technologies to interface with because of their 3V output signal. 3V ICs such as LVQ have input specifications similar to the 5V TTL or TTL-compatible CMOS ICs. In this case, interfacing at this point may be direct. To safeguard this configuration against voltage and temperature fluctuations the designer should regulate BOTH the 3.3V and 5V power supplies together. Another option is to purposely run the 5V power supply on the low side to decrease the 5V-3V VOHto-V_{CC} delta. This optimum configuration reduces any DC power loss from termination at the interface to zero. However, if the same system is allowed to operate with power supply tolerances that could vary ±10% independently (examples: 5.0V + 10% and 3.3V -10%), then the input specifications for LVQ products would be violated. In order to remain within the absolute maximum specifications for LVQ products, the VOH of the TTL I/O must be held to within 0.5V of the LVQ V_{CC}. The best way to reduce V_{OH} while retaining signal fidelity and specified propagation delays is to add a parallel resistor termination (to GND) to every signal line at the dual voltage interface.

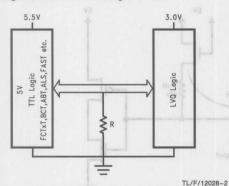


FIGURE 1a. Dual Voltage with Parallel Resistor Termination

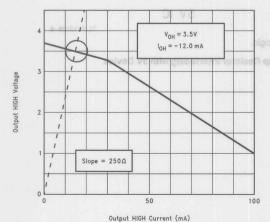


FIGURE 1b. 74F244 Output Drive

The "R" value in *Figure 1a, Figure 1b* is derived using manufacturer supplied I_{OH}/V_{OH} curves in conjunction with the formula: R = 3.5V/ I_{OH} @ V_{OH} = 3.5V. In this example, the bipolar I_{OH}/V_{OH} curve is from the FAST Applications Handbook. Although only the 74F244 case is shown, the method also applies to a "reduced swing" CMOS, BICMOS, and other bipolar devices.

2.0 Interfacing to Pure 3V LVQ

2.2 INTERFACING 5.0V CMOS TO PURE 3V LVQ LOGIC

When ordinary LVQ inputs are driven beyond V_{CC} , large currents will flow into the silicon substrate raising the internal V_{CC} of the device to 4.0V or above. Therefore, it is generally not recommended to interface CMOS at 5.0V to these devices at 3.3V. However, such a configuration may become unavoidable in some mixed/dual voltage designs. In order to reduce the V_{OH} level of a CMOS device, a voltage divider must be set up on the output to provide the correct V_{OH} level to the device. One possible configuration is shown in the *Figure 2*.

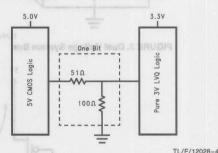


FIGURE 2. Dual Voltage with Resistor Divider Network

Although DC power is consumed by the voltage divider, using higher values of resistance for the voltage divider will create an additional propagation delay across the interface. This is due to the RC time constant setup by device inputs and the Thevenin equivalent resistance of the voltage divider. The resistance values shown exhibit a good compromise between DC power loss and signal fidelity.

2.3 INTERFACING PURE 3V LVQ LOGIC TO 5.0V INPUTS

Interfacing a 3V LVQ IC's output to a 5V TTL-compatible input can be done directly. LVQ 3V output specifications and 5V TTL-compatible specifications are compatible. Interfacing a 3V LVQ output to a 5V CMOS (VIH = 3.15V @ VCC = 5.0V) input should NEVER be done, because the 5V CMOS part will require a low impedance pull-up to VCC to satisfy its input requirements. Whenever a Pure 3V LVQ output is pulled up beyond its VCC, an intrinsic diode in the output structure will begin to forward bias causing excessive currents to flow from the interface through the 3V output and into the 3.3V power supply. This could raise the output level of the 3.3V supply to a level exceeding the maximum rated voltages for some low voltage devices.

Many types of 5V Bipolar inputs can present a similar problem at the dual voltage interface. It is common for a Bipolar device to have 10 k Ω –20 k Ω internal pull-up resistors on every input pin connected directly to the 5V V_{CC} plane. In this case, external pull-down resistors are recommended to create a voltage divider network that would set the logic HIGH voltage to a safe level for the 3V output as described earlier. *Figure 3* illustrates such an interface. This type of

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2.0 Interfacing to Pure 3V LVQ

Logic (Continued) t exupt at exupt of eulev "A" ent

pull-down is also ideal for any bus with Bipolar or "Reduced Swing" I/O that can be TRI-STATE with high-impedance driver outputs. In the past, busses of this type were pulled up to V_{CC} with $4~k\Omega$ resistors. The same results, pulling the bus away from threshold sensitive areas, are achieved with the pull-down resistor recommended. The value of this resistor is chosen based on the desired voltage divider network

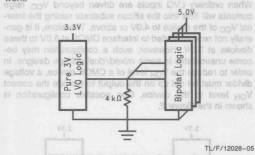


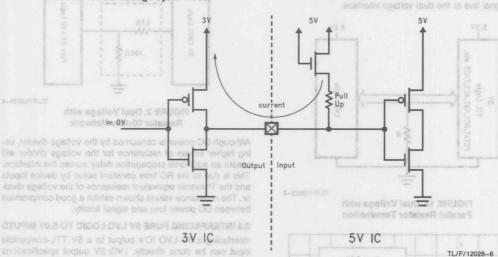
FIGURE 3. Dual Voltage System Bus

3.0 Interfacing to 5V Tolerant LVX S

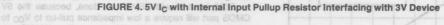
3.1 INTERFACING 5V TOLERANT OUTPUTS TO 5V BUSSES AND 5V DEVICES WITH INPUT PULL-UPS

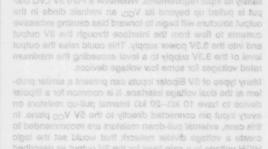
5V tolerant **inputs** may safely be connected to 5V busses, however, care must be taken when interfacing 5V tolerant **outputs** to 5V busses to make certain these outputs are always in TRI-STATE when a 5V signal exists on the bus. It is important to note that this 5V signal may not only arise from bus contention, but also a bus which is pulled up to $V_{CC}=5V$ by a pull-up resistor. A similar but less obvious situation which should be avoided occurs when these outputs are connected to 5V devices with input pull-up resistors. Devices, such as certain PLD's and chipsets which have internal input pullups will cause leakage currents to flow through the pull-up and into the substrate of the 3V device. Close attention should be paid to 5V device datasheets and 5V bus architectures to be sure no pull-ups exist.

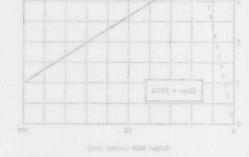
LVQ products, the V_{OH} of the TTL I/O must be hald to within 0.5V of the LVQ V_{OC}. The best way to reduce V_{OH} while retaining signal fidelity and specified propagation devalue to add a persible resistor termination (to GND) to every signal tipe at the dual voltage interface.



Caution: Avoid driving 5V IC's that have input pull-ups with 3V logic.







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FIGURE 1b. 74F244 Output Drive

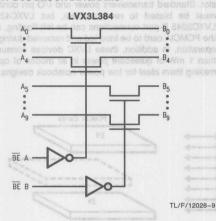
3.0 Interfacing to 5V Tolerant LVX and LCX Logic (Continued)

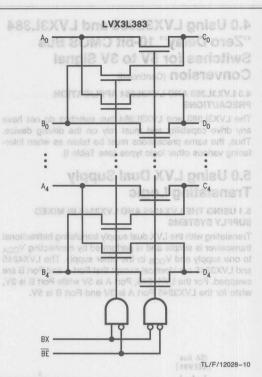
3.2 INTERFACING 5V TOLERANT LOGIC TO 5V CMOS INPUTS

Never interface a 3V "TTL compatible" output directly to a 5V CMOS (VI_H = 3.15V @ V_{CC} = 5.0V) input. The 3V IC cannot satisfy the VI_H requirement of the 5V CMOS input. If the 3V device is able to switch the 5V CMOS device, it will do so unreliably. A 5V translator with a higher V_{OH} such as the 74LVX3245 (V_{OH} = 4.4V @ I_{OUT} = $-100~\mu\text{A}$) should be used instead.

4.0 Using LVX3L383 and LVX3L384 "Zero Delay" 10-bit CMOS Bus Switches for 5V to 3V Signal Conversion

4.1 10-BIT BUS BLOCK DIAGRAMS





The 10-bit CMOS bus switches consist of NMOS pass transistors which act as a 5Ω switch between the two ports. Input signals are conveyed from one port to the other relatively unchanged except that they are clipped to a maximum voltage of about $V_{OUT\ MAX} = V_{CC} - 1V$ since the transistor begins to turn off as its source/drain nears its gate voltage. By adding a diode between the V_{CC} pin and a 5V supply, $V_{OUT\ MAX}$ is approximately $V_{CC} - 1.7V = 3.3V$. Thus, when 5V signals are applied to either port, they are clipped to about 3.3V. Substrate leakage issues are not a problem as they are with some 5V tolerant logic because the pass transitively included.

sistors are NMOS, not PMOS, devices. Thus, the source/drain to substrate intrinsic diode is reverse biased, not for-

4.2 ADDITIONAL BENEFITS OF USING LVX3L383 AND LVX3L384 5V TO 3V TRANSLATORS

The LVX3L383 and LVX3L384 provide 5V–3V translation while consuming almost no current (0.3 μ A) and having virtually no propagation delay (\leq 250 ps). In addition, the bus enable signals (which are tied to the transistors' gates) can be used to turn off the translation function to reduce switching power when in power conservation mode. The bus enable signals can also be used to increase the speed of some busses by disconnecting devices when they are not required to talk to the bus. This reduces the loading on the bus which can increase bus speeds.

ward biased.

4.0 Using LVX3L383 and LVX3L384 "Zero Delay" 10-bit CMOS Bus Switches for 5V to 3V Signal

Conversion (Continued)

4.3 LVX3L383 AND LVX3L384 APPLICATION PRECAUTIONS

The LVX3L383 and LVX3L384 bus switches do not have any drive capability and must rely on the driving device. Thus, the same precautions must be taken as when interfacing various other logic types (see Table I).

5.0 Using LVX Dual Supply Translating Logic

5.1 USING THE LVX4245 AND LVX3245 IN MIXED SUPPLY SYSTEMS

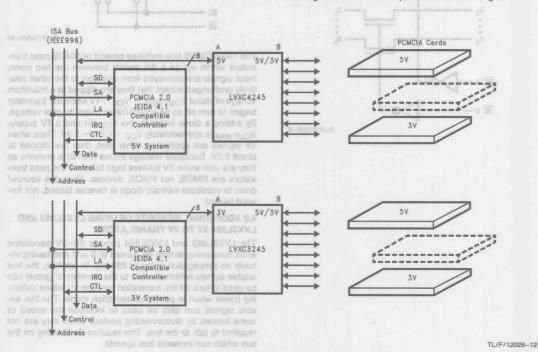
Translating with the LVX dual supply translating bidirectional transceiver is simple and is performed by connecting V $_{\rm CCA}$ to one supply and V $_{\rm CCB}$ to the other supply. The LVX4245 and LVX3245 are identical except that Port A and Port B are swapped. For the LVX4245, Port A is 5V while Port B is 3V, while for the LVX3245 Port A is 3V and Port B is 5V.

5.2 USING THE LVXC4245 AND LVXC3245 FOR PCMCIA CARD INTERFACE

The flexible PCMCIA 2.0 standard allows for both 3V and 5V PCMCIA cards as well as for supply voltage to be reduced from 5V to 3V for power conservation. Such requirements necessitate a configurable port-to-card interface design. National Semiconductor's LVXC4245 and LVXC3245 provide on demand B-port supply voltage configuration for PCMCIA card and other real time configurable I/O applications.

The A Port supply voltages for the LVXC4245 and LVXC3245 are 5V and 3V, respectively. The devices' B-ports are configurable by changing the supply voltage on the B-port V_{CC} pin. Changing the supply voltage on the B-port V_{CC} pin between 3V and 5V will configure the B-port I/O to either 3V or 5V I/O levels. Thus, for PCMCIA applications, 3V and 5V cards are accommodated by tying the B-port V_{CC} to the card voltage supply.

There are other PCMCIA port-to-card interface considerations. For instance, the B-port supply and I/O pins will float coincidentally when the PCMCIA card is removed from the slot. Standard transceivers power and I/O pin connections must be biased to remain active, but LVXC4245 and LVXC3245 B-port connections can be left floating, allowing the PCMCIA card to be inserted and removed during normal operation. In addition, these LVXC devices consume less than 1 mW of quiescent power in all modes of operation, making them ideal for low power notebook designs.



6.0 Summary

There are a variety of low voltage logic choices available to system designers. They can be classified into their level of 5V tolerance: pure 3V, 5V input-only tolerant, 5V input and output tolerant, bus switches, and dual supply 3V/5V translator logic devices. At first the choices and their interface requirements may seem confusing, but each has its own benefits:

Benefits of National Semiconductor's Low Voltage Logic

LVQ Octals, Gates, MSI 3V Inputs and Outputs Low Cost Low Power Reduced Noise Low EMI LVX Octals, Gates, MSI To depress of 5V Tolerant Inputs The value = Low Cost 1 = elgma2 to smill st Low Power and swall medical a Broad Family WaveW Instruct # LVX3L383/4 Bus Switch Family 5V-3V Translation "Zero Delay" (250 ps) 5V-3V Transition Ultra Low Power Consumption **LVX Translator Family** 5V-3V and 3V-5V Translation Efficient Translation Configurable B-Port (LVXC) Low Power was a trottonimet LCXnrt abnot loads. Loads that Vision or espe Octals, 16-bit enil ent to bne ent bns revib ent 5V Tolerant Inputs and Outputs High Speed charges and to acres and Low Power slumet ent of gnilbooce enil ent ±24 mA Drive Powerdown High Impedance series resistor) plus tire output impedance (ZcTVII Octals, 16-bit 5V Tolerant Inputs and Outputs Higher Speed vol bilay a gyispon lilw sail

Factors such as speed, power, cost, quantity and location of 3V logic on the board, and noise should be considered when choosing the appropriate logic family. National offers multiple alternate sourced low voltage logic families to choose from in order to provide cost effective, efficient, and reliable solutions in a variety of applications.

asmit dw/ (

Higher Drive (+64/-32 mA)

Busholdva agatlov liut ant see lilw stugni lis, and

Power up/down High Impedance

In mostly 3V systems, National's LVQ logic provides the most cost effective solution. The LVQ family offers a wide range of logic functions from transceivers to MSI devices. LVQ devices also feature very low power consumption and patented Quiet Series EMI reduction circuitry.

Line Driving and Termination (Continued)

LVX and LCX are recommended for interfacing between 3V and 5V signals. Both are based on a CMOS process. Because it is CMOS based, both consume very little power which make them ideal for battery powered applications. Both have guaranteed simultaneous switching noise level and dynamic threshold performance. This is where the similarity ends.

LVX is recommended for slower and more cost sensitive mixed supply systems. It has very low noise due to its lower drive capability. LVX can provide the majority of logic functions because it offers the broadest family line. It can tolerate 5V signals on its inputs which makes it ideal for interfacing 5V or 3V signals.

LCX is recommended for high speed applications. This is National's flagship CMOS line. It is built on our state-of-theart CMOS process. With a higher drive capability than LVX and National Semiconductor's patented Quiet Series EMI reduction circuitry a designer can now have the best of both worlds; low noise and high drive. It can not only tolerate 5V on its inputs and also on its outputs (or I/Os) when in TRI-STATE.

The LVX3L384 and LVX3L383 provide very fast, ultra low power translation from 5V to 3V signal levels. They can also be used to isolate signals in order to reduce switching power and bus loading.

In situations where there is a need for 3V/5V translation only, the LVX translator family provide the most reliable and efficient interface. Use the 74LVX4245 or 74LVX3245 where the supply voltages are fixed and use the LVXC4245 or LVXC3245 when it is necessary to select the B-port supply voltage on-the-fly.

In a bus/backplane environment (i.e., in telecommunication, PBx etc.) where power up/down high impedance is necessary or a high performance system (i.e., Workstations, servers etc.) where high drive or speed is required; LVT can provide the solution.

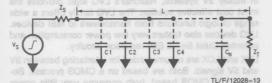
Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z'_{0} , the effective equivalent impedance of the line, and t_{pde} , the effective propagation delay down the line. It should be noted that the

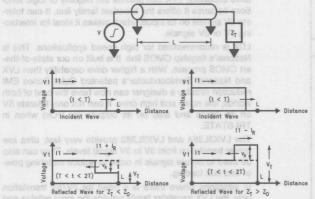
Line Driving and Termination (Continued)



Length of Transmission Line = L Distributed Load Capacitance per Unit Length = CD = Characteristic Impedance of a Transmission Line Altered by Distributed Loading

Effective Reflection Coefficient at Termination = p =

FIGURE 5a. Transmission Line with Distributed Loading



- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t
- Incident Wave Current = I₁
- Incident Wave Voltage = V₁
- Reflected Wave Current = I_R
- Reflected Wave Voltage = V_R
- Characteristic Impedance of Line = Z_O
- Termination Impedance = Z_T
- Voltage at Termination = V_T

TI /F/12028-14 FIGURE 5b. Reflections Due to Impedance Mismatching TV8-V8 bits V8-V8

SERIES TERMINATIONS

the line according to the formula

intrinsic values of line impedance and propagation delay, Zo and tpd, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z'o and tode can be calculated with:

$$Z'_{o} = \frac{Z_{o}}{\sqrt{1 + C_{D}/C_{L}}}$$

$$t_{ode} = t_{od}\sqrt{1 + C_{D}/C_{L}}$$

where C_L = intrinsic line capacitance and C_D = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave, Vi. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of

 $V_i = V_{DD} \bullet Z'_o / (Z'_o + R_S + Z_S)$

The amplitude will be one-half the voltage swing if Rs (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices

on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times

the delay of the line.

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

Line Driving and Termination (Continued) AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable.

The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

THEVENIN TERMINATION bas (0.1 = 12) his to strusterioo

his critical length is the ring its rise or fall time.

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle.

Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{DD} or ground, increasing power consumption.

■ Parallel: Resistor = Z_0 ■ Thevenin: Resistor = $2 \times Z_0$ ■ Series: Resistor = $Z_0 - Z_{out}$

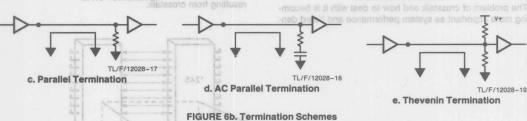
Resistor = Z₀

Noise Effects

FIGURE 6a. Suggested Termination Values



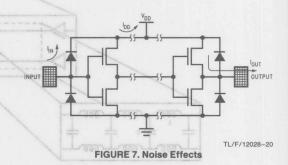
a. No Termination notes to the series Termination



CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to $V_{\rm CC}$ and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 7 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is HIGH. Depending upon the system, this current, $I_{\rm IN}$, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line. Another possible solution would be to ensure that the output enable input is inactive, preventing the outputs from turning on and loading down the bus. This may be accomplished by hardwiring a 4.7 k Ω pull-up resistor to the V_{CC} pin of the device.



Noise Effects

Low Voltage Logic offers excellent noise immunity.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the performance of Low Voltage Logic circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board den-

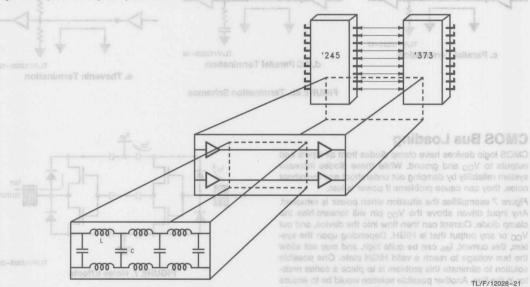
sities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent. See *Figure 8*.

Crosstalk has two basic causes. Forward crosstalk, *Figures 9* and *11*, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ($\epsilon_{\rm f}=1.0$) and epoxy glass ($\epsilon_{\rm f}=4.7$). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figures 10 and 12, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk.

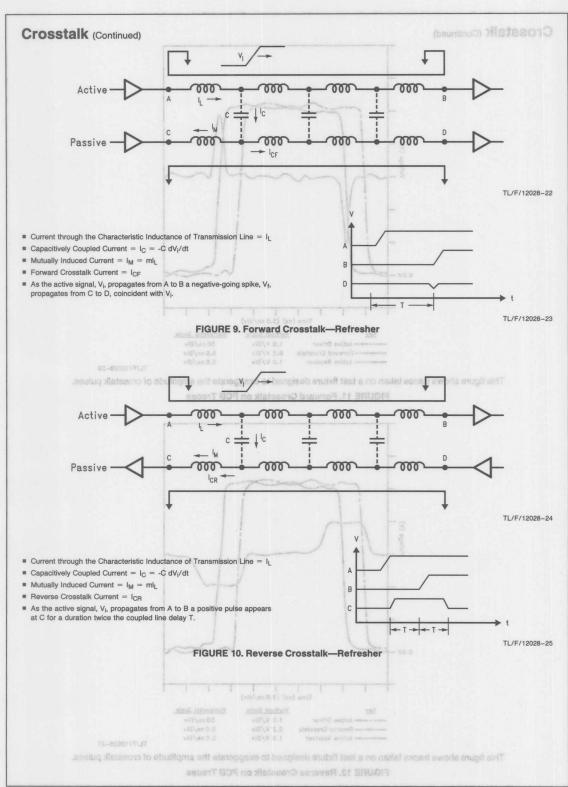
puts from turning on and loading down the bus. This may be



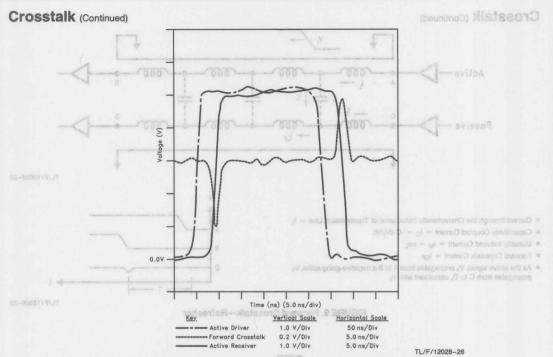
Two parallel signal lines provide mutual inductance and shunt capacitance.

FIGURE 8. Where Does Crosstalk Take Place? And Value printed and bedeligmones

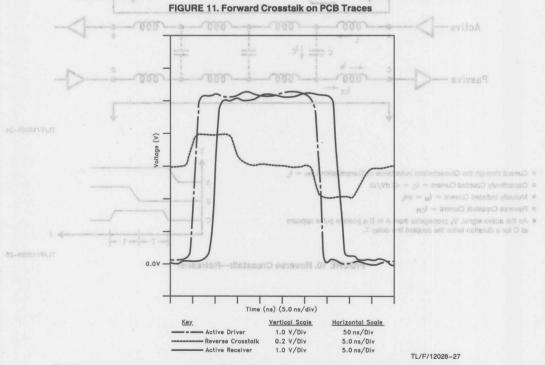
4-12







This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.



This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Crosstalk (Continued)

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. See Figure 13. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termina-

tion. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them. See *Figure 14*.

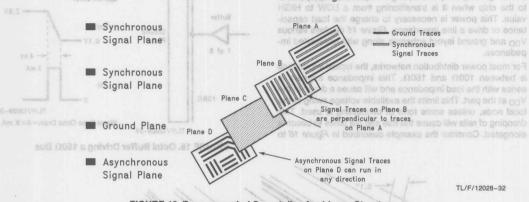
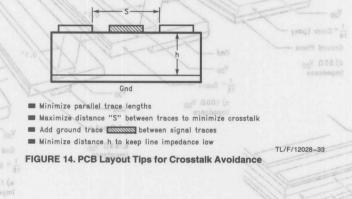


FIGURE 13. Recommended Crosstalk—Avoidance Structure



PIQUAE 16. Power Distribution impedances

Decoupling Requirements

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with Low voltage logic products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 15 displays various $V_{\rm DD}$ and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 100Ω and 150Ω . This impedance appears in series with the load impedance and will cause a droop in the V_{DD} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 16 to

calculate the amount of decoupling necessary. This circuit utilizes a '244 driving a 150 Ω bus from a point somewhere in the middle.

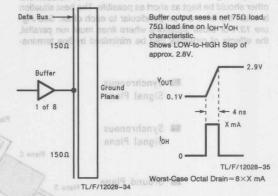


FIGURE 15. Octal Buffer Driving a 150 Ω Bus

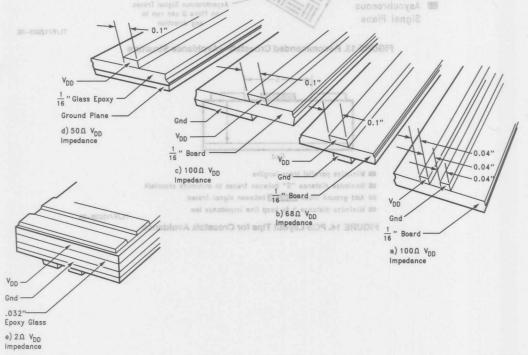


FIGURE 16. Power Distribution Impedances

TL/F/12028-36

Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 150Ω loads in parallel, or an effective impedance of 75Ω . To switch the line from rail to rail, a given drive of X mA is needed; more than X mA x 8 will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 17.

In this example the drive needed, if all 8 lines switch at once, is 300 mA, plus the V_{DD} droop is to be kept below 20 mV and the edge rate equals 4 ns, a 0.10 μF capacitor is needed

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package. See *Figure 18*.

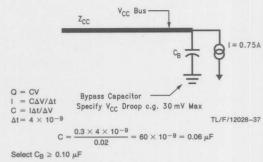
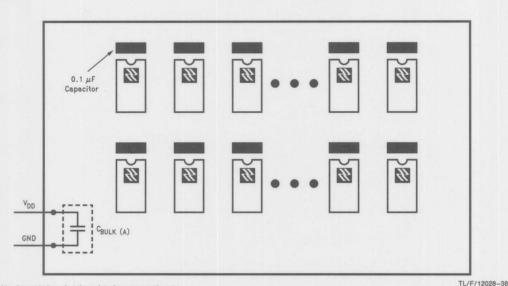


FIGURE 17. Formula for Calculating Decoupling Capacitors



- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 μF-100 μF)

FIGURE 18. Board-Level Decoupling Capacitor

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capaci-

tors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 1500 loads in parallel, or an effective impedance of 750. To switch the line more rail, a given drive of X mA is needed; more than X mA x 6 will be required if all eight lines which at once. This instanance current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage aroop will lengthen device rise and relect of the voltage aroop will lengthen device as and fall times and slow system operation. A local decoupling the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a mirrimum. The necessary values for decoupling capacitors can be celculated with the formula given in Fig. 17.

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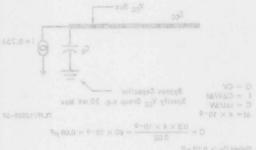


FIGURE 17, Formula for Calcu

CAND SELECTION OF SELECTION OF

- Need to decouple board at the point of power supply energy
- This capacifor (A) will smooth few frequency bulk switching noise
- A large value electrolytic capacitor is typically used (80 µF-100 µF)

FIGURE 18. Board-Level Decoupiing Capacitor

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitaminarily of series inductance and series resistance.

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Section 5 Contents

5-3	LCX Family Features
	74LCX240 Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs
	74LCX244 Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs
6-10	74LCX245 Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs
5-14	74LCX373 Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs
5-18	74LCX374 Low-Voltage Octat D Flip-Flop with 5V Tolarant Inputs and Outputs
5-22	74LCX646 Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs
	74LCX652 Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs
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	Inputs/Outputs
5-35	74LCX16244 Low-Voltage VilmaTrXOL river with 5V Tolerant inputs and Outputs 74LCX16245 Low-Voltage 15-Bit Bidirectional Transceiver with 5V Tolerant inputs and
	74LCX16245 Low-Voltage 15-Bit Bidirectional Transceiver with 5V Tolerant Inputs and
5-39	Outputs
5-43	74LCX16373 Low-Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs
	74LCX16374 Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs
	74LCX16646 Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs.
	74LCX16652 Low-Voltage Transcelver/Register with 5V Tolerant Inputs and Outputs

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ALAS SEMICONDUCTOR

LCX Low Voltage High Speed CMOS Logic with 5V Tolerant Inputs and Outputs

noticular IMENas Features leiuO betneting atnematical	Advantages Advantages
Extended V_{CC} range from 2.7V to 3.6V, compatible with VELOCION JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
Advanced 0.8 μm CMOS process	High performance with propagation delays as fast as 6.5 ns max for octals
No input-diode clamp to $\ensuremath{V_{CC}}.$ Advanced overvoltage circuit design techniques.	5V tolerant inputs and outputs. Interfaces directly to standard 5V buses and 5V devices.
Low standby current (I _{CC} 10 μ A max for octal over temp)	Saves power, extends battery life
Power down overvoltage protection	Device is protected at inputs and outputs if V _{CC} drops to zero volts
±24 mA drive current	Guaranteed incident wave switching into 50 $\!\Omega$ transmission lines
SOIC, EIAJ-SOIC, and TSSOP packaging	Saves board space and weight; TSSOP compatible with PCMCIA standards
Alternate sources available	Product standardization. Ensured product supply.

Outputs (Pins 3, 5, 7, 9)

der Number		7/LOX240MTCX
e NS Fackage Number		



PRELIMINARY

74LCX240

Low-Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs 90510V WO.

The LCX240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

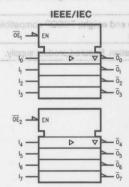
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications

General Description outputs

- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction
- Functionally compatible with the 74 series 240
- Latchup performance exceeds 300 mA
- ESD performance:

Human body model > 2000V; Machine Model > 250V anavbA . 20V of gmalo shoib-tug

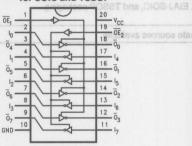
Ordering Code: See Section 11 15 1651 **Logic Symbol**



TL/F/11993-1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/11993-2

Pin Names	n Names Description			
\overline{OE}_1 , \overline{OE}_2 I_0-I_7 $\overline{O}_0-\overline{O}_7$	TRI-STATE® Output Enable Inputs Inputs Outputs			

Truth Tables

Inputs In		Outputs		
		(Pins 12, 14, 16, 18)		
L	L	Н		
L	Н	L		
H X		Z		

Inpu	its	Outpute	
OE ₂	In	Outputs (Pins 3, 5, 7, 9)	
L	L	Н	
L	Н	L	
Н	X	Z	

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LCX240WM 74LCX240WMX	74LCX240SJ 74LCX240SJX	74LCX240MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Office/ Distributors for availability	and specifications.
Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Voltage(V _I)	-0.5V to +7.0V
Output Voltage (Vo)	
Outputs Tri-stated	-0.5V to $+7.0V$
Outputs Active (Note 2)	$-0.5V$ to $V_{CC} + 0.5V$
DC Input Diode Current (I _{IK}) V _I < 0V	-50 mA
DC Output Diode Current (I _{OK}) V _O < 0V V _O < V _{CC}	-50 mA +50 mA
DC Output Source/Sink Current (I _{OH} DC V _{CC} or Ground Current	/I _{OL}) ±50 mA
per Supply Pin (I _{CC} or I _{GND})	±100 mA
Storage Temperature Range (TSTG)	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings.

The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Recommended Operating A Conditions

0 1 1/ 1	
Supply Voltage Operating Data Retention Only	2.0V to 3.6V 1.5V to 3.6V
Input Voltage (V _I)	0.0V to 5.5V
Output Voltage (Vo)	
Output in Active State	0V to V _{CC}
Output in "OFF" State	0.0V to 5.5V
Output Current I _{OH} /I _{OL} V _{CC} = 3.0V to 3.6V V _{CC} = 2.7V to 3.0V	±24 mA ±12 mA
Free Air Operating Temperature (T _A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$) $V_{IN} = 0.8V$ to 0.2, $V_{CC} = 3.0V$	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions
Syllibol			Min	Max	Units	Conditions
VIH	High Level Input Voltage	2.7-3.6	2.0	Sign	V	V _{OUT} ≤ 0.1V or
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8	utput Capapit	≥ V _{CC} - 0.1V
V _{OH}	High Level Output Voltage V	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2		ower Dissipati apacitance	
V _{OL}	Low Level Output Voltage	2.7-3.6 3.7 3.0		0.2 0.4 0.55	٧	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
l _l	Input Leakage Current	2.7-3.6		±5.0	μΑ	$0 \le V_I \le 5.5V$
loz	TRI-STATE Output Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$
loff	Power Off Leakage Current	0		100	μΑ	$V_I \text{ or } V_O = 5.5V$
Icc	Quiescent Supply Current	2.7-3.6		10	μΑ	$V_I = V_{CC}$ or GND
		2.7 0.0	JE-LY	±10	μΑ	$3.6 \le (V_I, V_O) \le 5.5$
Δlcc	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$

AC Electrical Characteristics: See Section 2 for Test Methodology 1587 mumixs M ethodology

Symbol	Parameter VCC	$T_A = -40^{\circ}\text{C to} + 85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$		
Va.Symbol	(v) perating Lata Relention Only Input Voltage (V)	-0.5V10 + 7.0V	Max (agV) epitleV ylqqu2 (Note 2) (West slov tugal 20	
t _{PHL}	Propagation Delay 2.7 Data to Output 2 2 2 3.0 - 3.6	1.5 V0.7 + of 1/5.0—	7.5 (oV) apstloV fuctuO ns 6.5 betsta nT atuqtuO	
t _{PZL}	Output Enable Time 2.7	Ve.0 + 21.50 Ve.0 - Am 08 - 1.5	Outputs Active (Note 0.9 DC Isnut Diode Current 0.8) V ₁ < 0V	
A TPHZ	Output Disable Time of V = 2.7	Am 02— 1.5 2.1 + 50 mA	8.0 7.0	
toshl toshh	Output to Output and the minimal of 3.0 Skew (Note 1). V. S. O. o. V. O. a. 3.0	lot) ±50 mA	DC Output Source/Sink Current (IOH) on Source Supund Current	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodologyed for blunds solved entit been

Symbol	Parameter	V _{CC} (V)	T _A = 25°C	Units	table are nanditions at the absorbed at the absorbed The "Recommended Operating Control
V _{OLP}	Quiet Output Maximum Dynamic VOL	3.3	0.8	ad V	$C_L = 50 \text{ pF, V}_{IH} = 3.3 \text{V, V}_{IL} = 0 \text{V}$
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

DC Electrical Characteristics

Capacitance

Symbol	Paramet	0.00	Typical		Units	Conditions	Symbol
OIN TO V1.0 ≥ TUOV	Input Capacit	ance	7 0.5	-	pF _{3.6-7.3}	V _{CC} = Open V _I = 0V or V _{CC}	нιν
Cout	Output Capac	itance	8		9.6-7.8 pF	V _{CC} = 3.3V lugnl evel wol	VIL
Au 001- = HO			S.0 -	Vec	2.7-3.6	VI = 0V or VCC UO avail ripli-	HOV
OH = -12 GqO H = -18 mA OH = -24 mA	Capacitance	ation	32 A.S		2.7 3.0 Pq 3.0	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$	
$OL = 100 \mu A$ $OL = 12 mA$ $OL = 24 mA$		0.2 0.4 0.55			2,7-3,6 3.7 3.0	Low Level Output Voltage	YOV
) ≤ V ₁ ≤ 5.5V	Au	0.8±			2.7-3.6	Input Leakage Current	
$0 \le V_0 \le 6.6V$ $V_I = V_{IH} \text{ or } V_{IL}$		±5.0			2.7-3.6	TRI-STATE Output Leakage	zol
V ₁ of V ₀ = 5.5V		100				Power Off Leakage Current	lore -
VI = VCC or GND	/ Ац	10			2.7-3.6	Quiescent Supply Current	
$3.6 \le (V_1, V_0) \le 5.5V_0$	Asq				U.D. T.A		
V _H = V _{CC} - 0.6V	Azu	500			2.7-3.6	Increase in Icc per Input	Alcc

74LCX244

Arr

Low-Voltage Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX244 contains eight non-inverting buffers with TRI-STATE® outputs. The device may be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver. The LCX244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7 to 3.6V applications

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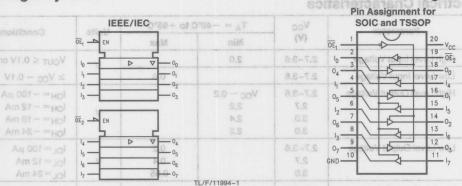
please contact the National Semiconductor Salas

- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 300 mA
- ESD performance: Human Body Model > 2000V; Machine Model > 250V

Ordering Code: See Section 11

Logic Symbol

Connection Diagram



Pin Names
Description

OE₁, OE₂
Inputs
O₀-O₇
Outputs

Truth Tables

V V Inpu	its An	Outputs	Inpu	its stranger	Outputs
ŌĒ ₁	In	(Pins 12, 14, 16, 18)	OE ₂	In land	(Pins 3, 5, 7, 9)
OC. IN.	L	L	L	L	L
L	Н	Н	L	Н	Н
Н	X	Z	H	X	Z

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX244WM 74LCX244WMX	74LCX244SJ 74LCX244SJX	74LCX244MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

TL/F/11994-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Output Diode Current (I_{OK}) $V_O < 0$ $V_O > V_{CC}$ DC Output Source/Sink Current (I_{OH}/I_{OL}) ± 50 mA = 50 mA = 50 mA = 50 mA

per Supply Pin (I_{CC} or I_{GND}) ±100 mA Storage Temperature Range (T_{STG}) -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Supply Voltage (V_{CC}) 2.0V to 3.6V Operating 1.5V to 3.6V **Data Retention Only** 0V to 5.5V Input Voltage (V_I) Output Voltage (VO) Output in Active State 0.0V to VCC Output in "OFF" State 0.0V to 5.5V Output Current IOH/IOL V_{CC} = 3.0V to 3.6V = 24 mA $V_{CC} = 2.7 \text{V to } 3.0 \text{V}$ Free Air Operating Temperature (T_A) -40°C to +85°C Minimum Input Edge Rate (Δt/ΔV) V\sn 01 3V) Vcc app $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$

DC Electrical Characteristics

Symbol	Symbol Parameter		$T_A = -40$	0°C to +85°C	Units	Conditions		
Symbol	or Parameter	(V)		Min Max		10 10 10	Conditions	
VIH	High Level Input Voltage	2.7-3.6	2.0	60-14 4	V	V _{OUT} ≤ 0.1V or		
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8		≥ V _{CC} - 0.1V		
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	0	> 3	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$		
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	A 4	I_{OL} = 100 μ A I_{OL} = 12 mA I_{OL} = 24 mA		
li I	Input Leakage Current	2.7-3.6	1-9681174	±5.0	μΑ	$0 \le V_I \le 5.5V$		
loz	TRI-STATE Output Leakage	2.7-3.6	TRI-STATE	35 ±5.0	μА	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$		
loff	Power Off Leakage Current	OV	Outputs	100	μΑ	$V_I \text{ or } V_O = 5.5V$		
Icc	Quiescent Supply Current	2.7-3.6		10	μΑ	$V_I = V_{CC}$ or GND		
at	outs Outpu	0.0	1000	± 10	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$		
Δlcc	Increase in I _{CC} per Input	2.7-3.6	701.70	500	μΑ	$V_{IH} = V_{CC} - 0.6V$		

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Logic Symbols

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AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol Parameter	Bouwator	V _{CC}	$T_A = -40^\circ$ $C_L =$	Units	
	Parameter	(V)	Min	Max (Note 2)	PALCX
t _{PHL}	Propagation Delay Data to Output	2.7 3.0–3.6	1.5 1.5	7.5 6.5	ns
t _{PZL}	Output Enable Time	2.7 3.0–3.6	1.5 1.5	0.8 on	I in yens of
t _{PHZ}	Output Disable Time	2.7 3.0–3.6	Ineno 1.5 rol bebri	ATE® out 8.0 to \$150 ATE out 10 A	rs with TRI-ST sh TRI-ST d application
toshl, toslh	Output to Output Skew (Note 1)	outputs 3.0 Outputs	f intertacing to a 5V mines the direction incut dischase both	locations with capability tent. The '0.1 input deta	3.3V) V _{OC} app gna 2n nvironr late flow the

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	rmance: Human Book Model > 2000V;	Vcc	T _A = 25°C	Units	Conditions
Symbol	Parameter V03S < lebox	9:(V) BV	Typical	Units	Conditions
VOLP	Quiet Output Maximum Dynamic VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

Capacitance Capacitance

Symbol	Dear bus Of Parameter	Typical	Units	Conditions
C _{IN}	Input Capacitance	7 (A	50 PF.	$V_{CC} = Open$ $V_I = 0V \text{ or } V_{CC}$
Cout	Output Capacitance	8	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
CPD	Power Dissipation Capacitance	VS 4		$V_{CC} = 3.3V$
- B ₅	B ₁	32	pF	$V_I = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$

Description	Pin Names
Output Enable Input	
	Ac-A7
Side & Inputs or TRI-STATE Outputs	

dopo of

T3SOP JEDEC	SOIC EIAJ	SOIC-JEDEC	
74LCX245MTCX	74LCX245SJ 74LCX245SJX	74LCX245WM 74LCX245WMX	Order Number
		M20B	See NS Package Number



PRELIMINARY COMPANIENCE See Section 2 for Test Method

74LCX245

Low-Voltage Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX245 contains eight non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The T/\overline{R} input determines the direction of data flow through the device. The \overline{OE} input disables both the A and B ports by placing them in a high impedance state.

The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

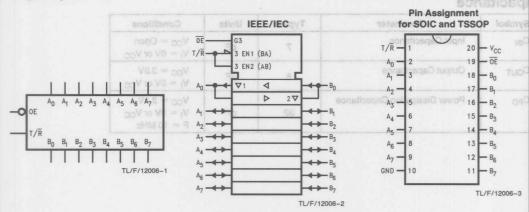
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 245
- Latch performance exceeds 300 mA
- ESD performance: Human Body Model > 2000V; Machine Model > 250V

Ordering Code: See Section 11

Logic Symbols

Connection Diagram

Syn



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Pin Names	Description
ŌĒ	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs
Bo-B7	Side B Inputs or TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX245WM 74LCX245WMX	74LCX245SJ 74LCX245SJX	74LCX245MTCX
See NS Package Number	M20B	M20D	MTC20

Absolute Maximum Ratings (Note 1) Truth Table: lise of the Truth Table: If the T If Military/Aerospace specific Inputs Outputs please contact the Mational OE T/R YEAC DR. Bus B₀-B₇ Data to Bus A₀-A₇ VoitHge (V Bus A₀-A₇ Data to Bus B₀-B₇ HIGH Z State on A₀-A₇, B₀-B₇ XV H = High Voltage Level L = Low Voltage Level = Immaterial = Immateria. = High Impedance + 50 mA Logic Diagram Vo.E = 30V, Vo.S of Vo.0 = 1/11V beyond which the safety of the device table are not quaranteed at the absolute 1 of 8 TL/F/12006-4

orana (Massace)	- atual	to +65°C	0'08 AT	Vac		lodmy8
Conditions	ethiu -	205.74	niisi	(9)	Parameter	
	V			2.7-3.8	High Level Input Voltage	
V1.0 - 0.1V ≤	, T	8.0		2.7-3,6	Low Level Input Voltage	
$l_{OH} = -100 \mu A$ $l_{OH} = -12 mA$ $l_{OH} = -18 mA$ $l_{OH} = -24 mA$	٧		Voc - 0.2 2.2 2.4 2.4	2.7-3.6 2.7 3.0 3.0	High Level Output Voltage	
lot = 100 µA lot = 12 mA lot = 24 mA	V	0.2 0.4 0.66		2.7-3.6 2.7 3.0	Low Level Output Voltage	
$0 \le V_l \le 5.5V$	Au	0.0±		2.7-3.6	Input Leakage Current @ OE, T/R	
$0 \le V_{Cl} \le 6.5V$ $V_{I} = V_{IH} \text{ or } V_{IL}$	Aq	±6,0	la dia	2.7-3.6	TRI-STATE I/O Leakage	
	Ац				Power Off Leakage Current	
$V_1 = V_{OC}$ or GND	Ац	10		2.7-3.6	Quiescent Supply Current	
$3.6 \leq (V_b, V_C) \leq 5.5V$	Aq			1.50		
$V_{0.0} - g_{0.0}V = H_{0.0}V$		500			Increase in Icc per Input	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})

DC Input Voltage (V_I)

Output Voltage (V_O)

Supply Voltage (V_O)

A = 0.5V to +7.0V -0.4 at Input Voltage (V_I)

Output Voltage (V_O)

Outputs Tri-Stated -0.5V to +7.0VOutputs Active (Note 2) -0.5V to $V_{CC} + 0.5V$

DC Input Diode Current (I_{IK}) $V_I < 0$ —50 mA

DC Output Diode Current (IoK) $\begin{array}{c} V_O < 0 \\ V_O > V_{CC} \end{array} \qquad \begin{array}{c} -50 \text{ mA} \\ +50 \text{ mA} \end{array}$

DC Output Source/Sink Current (I_{OH}/I_{OL})
DC V_{CC} or Ground Current

per Supply Pin (I_{CC} or I_{GND}) ± 100 mA

Storage Temperature Range (T_{STG}) —65°C to +150°C Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Output in Active State 0V to V_{CC}
Output in "OFF" State 0V to 5.5V

 $\begin{array}{lll} \text{Output Current I}_{OH}/I_{OL} \\ \text{V}_{CC} = 3.0 \text{V to } 3.6 \text{V} & \pm 24 \text{ mA} \\ \text{V}_{CC} = 2.7 \text{V to } 3.0 \text{V} & \pm 12 \text{ mA} \end{array}$

Free Air Operating Temperature (T_A) -40°C to +85°C

Minimum Input Edge Ratge ($\Delta t/\Delta V$) $V_{IN}=0.8V$ to 2.0V, $V_{CC}=3.0V$

DC Electrical Characteristics

Symbol	Beremeter	Vcc	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Helte	Odial
	Parameter	(V)	Min	Max	Units	Conditions
VIH	High Level Input Voltage	2.7-3.6	2.0		V	V _{OUT} ≤ 0.1V or
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8	7	≥ V _{CC} - 0.1V
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2		V	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{mA}$ $I_{OH} = -18 \text{mA}$ $I_{OH} = -24 \text{mA}$
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
l _l	Input Leakage Current @ OE, T/R	2.7-3.6		±5.0	μΑ	$0 \le V_I \le 5.5V$
loz	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$
loff	Power Off Leakage Current	0		100	μΑ	$V_1 \text{ or } V_0 = 5.5V$
Icc	Quiescent Supply Current	2.7-3.6		10	μΑ	V _I = V _{CC} or GND
		2., -0.0		±10	μΑ	$3.6 \le (V_1, V_0) \le 5.5V$
ΔICC	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$

±50 mA

toshl,	Output to Output Skew (Note 1)		puts for bus brganized system app designed for low voltage 0:13V) V _{OC} bility of interfaction to a 5V signal as
	defined as the absolute value of the difference between the blies to any outputs switching in the same direction, either HIGH		
	ximum AC limits are design targets. Actual performance will be		
	Implements patented Quiet Series noise/EMI red		
Dynami	c Switching Characteristics: se	ee Section 2 for Test Methodolo	ogy
Symbol	Parameter V _{CC}	T _A = 25°C Units	Conditions

Min

1.5

1.5 1.5

1.5

THI-STA 6.1 out

1.5

Max (Note 2)

8.0

9.5 8.5

raists of c6.7t latelies

10 8.5 10890

Logic Symbols

7.0

Symbol	Parameter	VCC	T _A = 25°C	Units	Conditions
Symbol	mance:	(V) 8	Typical	Onits	Conditions
VOLP	Quiet Output Maximum Dynamic VOL	3.3	0.8	V	$C_{L} = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$
VOLV	Quiet Output Minimum Dynamic VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	S Input Capacitance	7 DBINE	pF	$V_{CC} = Open$ $V_{I} = 0V \text{ or } V_{CC}$
C _{I/O}	Input/Output Capacitance	8	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
C _{PD}	Power Dissipation Capacitance	32	pF ₉ 0	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$

2.7

3.0-3.6

2.7 3.0-3.6

2.7

3.0-3.6

Propagation Delay

 A_n to B_n or B_n to A_n

Output Enable Time

Output Disable Time

tPHL

tpLH

tPZL

t_{PZH}

tPHZ

tPLZ

Capacitance

	Pin Names
	C0-D7
Letch Enable Input	

TBSOP JEDEC	SOICEIAL	
74LCX373MTCX	74LCX373SJ 74LCX373SJX	
MTC20	CIOSM	



YRANIMIJARG COLONISTICS: See Section 2 for Test Methodology

Symbol

Symbol

74LCX373

Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX373 consists of eight latches with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

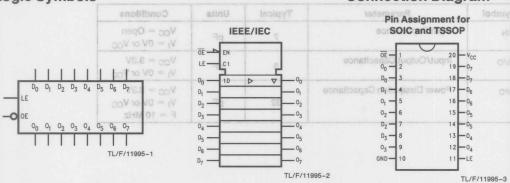
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 373
- Latchup performance exceeds 300 mA
- ESD performance:

Human Body Model > 2000V Machine Model > 250V

Ordering Code: See Section 11

Logic Symbols

Connection Diagram



Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
ŌĒ	Output Enable Input
00-07	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	
Order Number	74LCX373WM 74LCX373WMX	74LCX373SJ 74LCX373SJX	74LCX373MTCX	
See NS Package Number	M20B	M20D	MTC20	

Functional Description

The LCX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable (OE) input. When OE is LOW, the standard outputs are in the 2-state mode. When OE is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

VIN = 0.8V to 2.0V, Voc = 3.0V

Absolute Maximum Ratifelder Truth Table its Maximum Ratifelder Truth Table its Maximum Ratifeld Tru

re required, actor Sales	Inputs	lace specimentine Mational	Outputs
iffice agns.	In a Special	della Danol e	files/fortbutor
X 7.0V	Н	X	upply Valage (Vo
SV to H 7.0V	0- L	L (1	C Input Yoltage (V
H	L	н	ov) egst AV tudtul
EA 10 7-1.0A	0-L	X	Output O

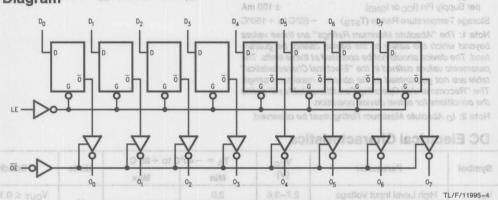
- H = HIGH Voltage Level L = LOW Voltage Level
- Z = High Impedance X = Immaterial

±50 mA

O₀ = Previous O₀ before HIGH to LOW transition of Latch Enable

DC Output Source/Sink Current (IGH/IGL)

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

$l_{OH} = +100 \mu A$ $l_{OH} = -12 mA$ $l_{OH} = -18 mA$ $l_{OH} = -18 mA$ $l_{OH} = -24 mA$			V ₀₀ - 0.2 2.2 2.4 2.2	2.7-3.6 2.7 3.0 3.0	High Lavel Output Voltage	
$l_{OL} = 100 \mu A$ $l_{OL} = 12 mA$ $l_{OL} = 24 mA$		0.2 4.0 0.55		2,7-3.6 2.7 3.0	Low Level Output Voltage	VOL
0 ≤ V ₁ ≤ 6.5V	Ащ				Input Leakage Current	
$0 \le V_0 \le 5.5V$ $V_1 = V_{1H} \text{ or } V_{1L}$				2.7-3.6		
				0	Power Off Leakage Current	
V _I = V _{CC} or GND				2.7-3.6	Quiescent Supply Current	
				0.0 1.0		
$V_{IH} = V_{CC} - 0.6V$		500		2.7-3.6	Increase in Icc per Input	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Office, Distributors for	avanability	and opcomodition
Supply Voltage (V _{CC})	V	-0.5V to $+7.0$ V
DC Input Voltage (V _I)		-0.5V to $+7.0V$
Output Voltage (V _O) Outputs TRI-STATE Outputs Active (Note 2	N X 2)	-0.5V to +7.0V -0.5V to V _{CC} + 0.5V
DC Input Diode Current ($I_{IK}) V_I < 0$	level egallov - 50 mA
DC Output Diode Currer $V_O < 0$ $V_O > V_{CC}$. 0.0	-50 mA +50 mA
DC Output Source/Sink	Current (IOH	/lol) ±50 mA

DC Output Source/Sink Current (IOH/IOL) DC Vcc or Ground Current

per Supply Pin (I_{CC} or I_{GND}) ±100 mA Storage Temperature Range (T_{STG}) = -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The

Recommended Operating another F The LOX373 contains eight D-two tatches enditions

Conditions
Supply Voltage dend dotal and narrow atuquo brabasta
Operating 2.0V to 3.6V
Data Retention Only 1.5V to 3.6V
Input Voltage (V _I) 0V to 5.5V
Output Voltage (Vo) of proceeding the (Vo) setup to the Output Voltage (Vo)
Output in Active State
Output in "OFF" State ON all on a Justice of OV to 5.5V
Output Current IOH/IOL 2-S and ni ens afuquo bisbinsta and
V _{CC} = 3.0V to 3.6V and mean studing brobasts a ± 24 mA
$V_{CC} = 2.7V$ to 3.0V alone disa evaluation and ± 12 mA
Free Air Operating Temperature (T _A) -40°C to +85°C
Minimum Input Edge Ratge (Δt/ΔV)
$V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$ 10 ns/V

parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation. Note 2: Io Absolute Maximum Rating must be observed.

DC Electrical Characteristics

O b a l	9 9 91	Vcc	$T_A = -40^{\circ}$	C to +85°C	Unite	Anna divisor		
Symbol	Parameter	(V)	Min	Max	Units	Conditions		
VIHREIMAN	High Level Input Voltage	2.7-3.6	2.0		V	V _{OUT} ≤ 0.1V or		
V _{IL}	Low Level Input Voltage	2.7-3.6	nego pigal to galbastere	0.8	diagnitin is prov	≥ V _{CC} - 0.1V		
V _{OH}	High Level Output Voltage	High Level Output Voltage 2.7-3.6 2.7 3.0 3.0	2.7 2.2 3.0 2.4	2.2 2.4		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OH} = -18 mA$ $I_{OH} = -24 mA$	
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$		
I	Input Leakage Current	2.7-3.6		±5.0	μΑ	$0 \le V_1 \le 5.5V$		
loz	TRI-STATE Output Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$		
I _{OFF}	Power Off Leakage Current	0		100	μΑ	V_{I} or $V_{O} = 5.5V$		
Icc	Quiescent Supply Current	2.7-3.6		10	μΑ	$V_I = V_{CC}$ or GND		
		2.7 -0.0		±10	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$		
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$		

ns

ns

Logic Symbols

Symbol	Parameter	V _{CC} (V)	T _A = -	Units	
			Min	Max (Note 2)	OVALLS
t _{PLH}	Propagation Delay D _n to O _n	2.7 3.0–3.6	1.5	9.0 1810 8.0 9081	oV-nso-
t _{PLH}	Propagation Delay LE to O _n	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t _{PZH}	Output Enable Time	2.7 3.0–3.6	1.5 1.5	9.5	I le lens
t _{PHZ} oileoilgq	w powe amil aldering the state overvoltage protection on	2007	TAI-SE.TE® o	bns qoll-q 8.50se not stu d A anot7.5 ngs bathe	no-aud ns all
ts	Setup Time	2.7 3.0–3.6		ore (JE) are common to ned for low-voltage (3,3V) interfacing to a 5V signi	
SOP H	SOIC JEDEC, SemiT blothed To	3.0-3.6		spricated with an advance high speed operation	sveirios ns. / y

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Specification applies to any outputs switching in the same shocker, such that it is seen to see the same shocker.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

2.7

3.0-3.6

3.0

4.0

4.0

1.0

Dynamic Switching Characteristics: See Section 2 for Test Methodology

LE Pulse Width

Output to Output Skew

(Note 1) 0000 < leboh yb

AC Electrical Characteristics: See Section 2 for Test Methodology

Cumbal	Pin Assignment for	Vcc	T _A = 25°C	11-14-	Conditions	
Symbol	90387 Parameter	(V)	Typical	Units		
VOLP	Quiet Output Dynamic Peak VOL	3.3	0.8	- 30 V	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	
VOLV	Quiet Output Dynamic Valley VOL	3.3	0.8	٧	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	

Capacitance

tw

toshL,

toslh

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	Input Capacitance	80 7	pF	V _{CC} = Open V _I = 0V or V _{CC}
C _{OUT}	Output Capacitance	12	pF 10	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
C _{PD}	Power Dissipation Capacitance	32 G	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$

Note 1: Guaranteed by design.

TSBOP JEDEC	SOIC EIAJ	SOIC JEDEC	
74LCX374MTCX		74LCX374WM 74LCX374WMX	Order Number
MTC20	M20D	BOSM	See NS Package Number



YARNIMIJAR acteristics: See Section 2 for Test Methodology

74LCX374

Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and TRI-STATE® outputs for bus-oriented applications. A buffered clock (CP) and Output Enable (OE) are common to all flip-flops. The LCX374 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

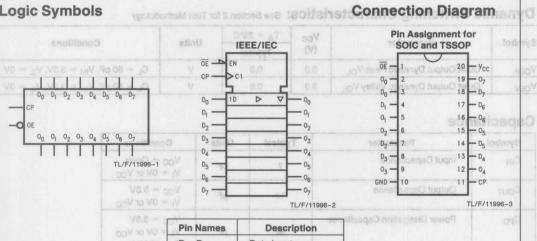
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications

Output Enable Time

- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction
- Functionally compatible with the 74 series 374
- Latchup performance exceeds 300 mA
- ESD performance:

Human Body Model > 2000V Machine Model > 250V

Ordering Code: See Section 11 **Logic Symbols**



Pin Names	Description
D ₀ -D ₇	Data Inputs
CP	Clock Pulse Input
ŌĒ	Output Enable Input
00-07	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC	
Order Number	74LCX374WM 74LCX374WMX	74LCX374SJ 74LCX374SJX	4SJX 74LCX374MTCX	
See NS Package Number	M20B	M20D	MTC20	

Functional Description

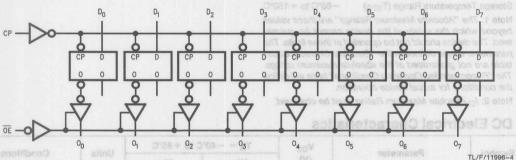
The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{\text{OE}}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops.

Truth Table is R mumikeM stuloadA

required uctor Sales	ospace apacity	Outputs	
Dn	OGE CP VOIL	Jalin OE of at of	odini On collifo
SV toH 7.0V	1	L (00V)	Shibbly Aldans
VO.THLOFVE	0- /	L (N) a	DC Input_Voltage
X	L	L (gV)	egaloo suque
SV X 7.0	X	H BTATE	BART ZughuO

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance
- / = LOW-to-HIGH Transition
- O₀ = Previous O₀ before HIGH to LOW of CP

Logic Diagram



TL/F/11996-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

				2.7-3,6	Low Level Input Voltage	
4 = -100 µA 4 = -12 mA 4 = -18 mA 4 = -24 mA	101	V	V ₀₀ - 0.2 2.2 2.4 2.2	2.7-8.6 2.7 3.0 3.0		
= 100 µA = 12 mA = 24 mA		V		2.7-2.6 2.7 2.0	apsticl/fuqtuO leve.J wo.J	
		Asq		0		
= Voc or GND					Quiescent Supply Current	
		Au				
		Au				

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V

Supply voltage (vCC)	0.54 10 1 7.04
DC Input Voltage (V _I)	-0.5V to $+7.0V$
Output Voltage (V _O) Outputs TRI-STATE Outputs Active (Note 2)	-0.5V to +7.0V -0.5V to V _{CC} + 0.5V
DC Input Diode Current (I _{IK}) V _I < 0	50 mA
DC Output Diode Current (IOK)	isinatammi = X
V _O < 0	-50 mA
V _O > V _{CC}	+ 50 mA
DC Output Source/Sink Current (IOH	/I _{OL}) ±50 mA

DC V_{CC} or Ground Current

Supply Voltage (Voc)

per Supply Pin (I_{CC} or I_{GND}) \pm 100 mA Storage Temperature Range (T_{STG}) -65° C to $+150^{\circ}$ C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Recommended Operating and John Tondon Conditions

Onland on office and on the second
Supply Voltage STATS-IRT and studie of operating of Ope
Data Retention Only W 3001-011 100 911 1.5V to 3.6V
Input Voltage (V _I) 0V to 5.5V
Output Voltage (Vo) Output in Active State Output in "OFF" State Ov to 5.5V
Output Current IOH/IOL state and facilities and acob fugat 30
$V_{CC} = 3.0V \text{ to } 3.6V$ $\pm 24 \text{ mA}$
$V_{CC} = 2.7V \text{ to } 3.0V$ ± 12 mA
Free Air Operating Temperature (T _A) -40°C to +85°C
Minimum Input Edge Ratge (Δt/ΔV)
$V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$ 10 ns/V
SARAN SALEMENT OF THE SALEMENT

DC Electrical Characteristics

O	Parameter	Vcc	$T_A = -40^{\circ}C$	to +85°C	Halte	Conditions
Symbol		(V)	Min	Max	Units	Conditions
VIH	High Level Input Voltage	2.7-3.6	2.0		V	V _{OUT} ≤ 0.1V or
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8	V	≥ V _{CC} - 0.1V
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2		٧	$I_{OH} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OH} = -18 mA$ $I_{OH} = -24 mA$
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	٧	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
l _l	Input Leakage Current	2.7-3.6		±5.0	μΑ	$0 \le V_{\parallel} \le 5.5V$
loz	TRI-STATE Output Leakage	2.7-3.6		±5.0	μА	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$
loff	Power Off Leakage Current	0		100	μΑ	$V_I \text{ or } V_O = 5.5V$
Icc	Quiescent Supply Current	2.7-3.6		10	μΑ	$V_I = V_{CC}$ or GND
		2.7 -0.0		±10	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	Vcc	$T_A = -4$	Units		
		(V)	Min	Max (Note 2)	WO II	
t _{PHL}	Propagation Delay CP to Output	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns	
t _{PZH}	Output Enable Time	2.7 3.0–3.6	uO bd.5 eiuc	9.5 8.5	ns	
t _{PHZ}	Output Disable Time	2.7 3.0–3.6	1.5 stiuo1.5 aviecans	10 8.5 10290 of succession 2.5 to africance	ns abaxas	
t _s another bris and	Setup Time Sesion wolves	2.7 3.0–3.6	2.5 2.5		at being to	
t _H	link 24 mA smiT bloH Itaneous switching noise level	2.7 3.0–3.6	WO.1.5t no treft (A891.510 BA90)	declinto the respective registion of the appropriate pin-	nol ed like at	
tw notion	Pulse Width bas 03030 to 1813\esion seles telu0 beir	2.7 3.0–3.6	4.0	e if through Figure 4. designed for tow voltage (3)	ns is	
toshl,	Output to Output Skew (Note 1)	Functionelly com	a -notivne langis V	a s of galasthetri to villide 1.0	ons with cap engen	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Overhal SS	IS19810 (Parameter 1100)	Vcc	T _A = 25°C	Helte	Conditions 2 0100	
Symbol		(V)	Typical	Units		
VOLP	Quiet Output Dynamic Peak VOL	3.3	0.8	٧	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	
V _{OLV}	Quiet Output Dynamic Valley VOL	3.3	0.8	V-	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	

Capacitance

Symbol		Parameter		Typical	Units	Conditions	
C _{IN}	00 10	03 Input	Capacitance	3-41	7 8	pF	$V_{CC} = Open$ $V_{I} = OV \text{ or } V_{CC}$
COUT	- B ₂	Outpu	t Capacitance	J4 -44-3	8	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
C _{PD}	8 - 8 ₅		r Dissipation Capac	itance	32	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$



YRANIMILER CLERISTICS: See Section 2 for Test Methodology

Parameter

Symbol

COSHL

74LCX646

Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in Figure 1 through Figure 4.

The LCX646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

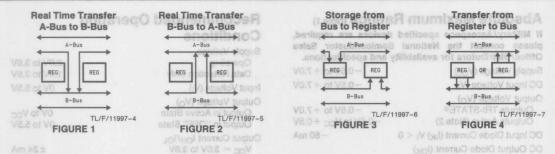
The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 646
- Latch performance exceeds 300 mA
- ESD performance; ent to aulay stulpeds ent as bentleb at wexl2 :
- write maintaining of the Human body Model > 2000V we shipto you of adapt notice to refusione many ballongs a Machine Model > 250V miles as shipto you of a muritisen will of

Dynamic Switching Characteristics: See Section 2 for Test Me Ordering Code: See Section 11 **Logic Symbols** Connection Diagram (V) Pin Assignment for SOIC and TSSOP IEEE/IEC 3 EN1 (BA) CPAB -3 EN2 (AB) SAB -23 - CPBA ►C4 CPAB DIR -- SBA SAB CPAB. 2139 — G 21 CPB/ 5 dioeas O tuani 20 -- B₀ ≥1 2∇ B1 B2 B3 B4 B5 B6 B7 7onneO tuotuO 18 - B₂ A3 -TL/F/11997-- B4 A5 -A6 -10 15 - B₅ **Pin Names** Description A7 -11 - B₆ Data Register A Inputs A0-A7 GND . 13 - B₇ Data Register A Outputs Data Register B Inputs B₀-B₇ TL/F/11997-3 Data Register B Outputs CPAB, CPBA Clock Pulse Inputs SAB, SBA Transmit/Receive Inputs TL/F/11997-2 G Output Enable Input DIR **Direction Control Input** SOIC JEDEC **TSSOP JEDEC** 74LCX646WM Order Number 74LCX646WMX 74LCX646MTCX See NS Package Number M24B MTC24





Function Table (Note)

		li	nputs	Edge Re	um Inout i	Data I/On oa ±		(Jol\Hol) Function 2\earus tuqtuo o
Gn 0	DIR	CPAB	V CPBA	SAB	SBA	A ₀ -A ₇	B ₀ -B ₇	C Voc or Ground Current
H H	X X X	H or L X	H or L	X X X	X X X	Input	Input to service a	Isolation Clock An Data into A Register Clock Bn Data into B Register
L L L	H H H	X Hor L	X X X	L H H	X X X	Input	gueran- nife. The tuqtuO ratings.	A _n to B _n —Real Time (Transparent Mode) Clock A _n Data into A Register A Register to B _n (Stored Mode) Clock A _n Data into A Register and Output to B _n
L L L	L L L	X X X	X H or L	X X X	L H H	Output	Input	B _n to A _n —Real Time (Transparent Mode) Clock B _n Data into B Register B Register to A _n (Stored Mode) Clock B _n Data into B Register and Output to A _n

Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

= LOW-to-HIGH Transition H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level High Level Input Voltage **Logic Diagram** Low Level Input Voltage High Level Output Voltage Am 81 CPBA Am AS - SBA -Au COL Low Level Output Voltag Am St = Jol Am as = 1 OF 8 CHANNELS Input Leakage Current TRI-STATE I/O Leakar Power Off Leakage Cu Quiescent Supply Curt Va.0 - 20 40-7 € Increase in I 200 TO 7 OTHER CHANNELS TL/F/11997-8

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5-23

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

 Supply Voltage (V_{CC})
 −0.5V to +7.0V

 DC Input Voltage (V_I)
 −0.5V to +7.0V

 Output Voltage (V_O)
 −0.5V to +7.0V

Outputs TRI-STATE® -0.5V to +7.0V Outputs Active (Note 2) -0.5V to $V_{CC} +0.5$ V DC Input Diode Current (I_{IK}) V_I < 0 -50 mA

DC Output Diode Current (I_{OK})

 $V_{\rm O} < 0$ —50 mA $V_{\rm O} > V_{\rm CC}$ +50 mA DC Output Source/Sink Current (I_{OH}/I_{OL}) ±50 mA

DC V_{CC} or Ground Current
per Supply Pin (I_{CC} or I_{GND}) ± 100 mA

Storage Temperature Range (T_{STG}) -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Supply Voltage
Operating
Data Retention Only
Input Voltage (V_I)

2.0V to 3.6V 1.5V to 3.6V 0V to 5.5V

Output Voltage (V_O)
Output in Active State
Output in "OFF" State

0V to V_{CC} 0V to 5.5V

Output Current I_{OH}/I_{OL} $V_{CC} = 3.0V$ to 3.6V $V_{CC} = 2.7V$ to 3.0V

±24 mA (etot/) Old & T cross ± 12 mA

Free Air Operating Temperature (T_A) Minimum Input Edge Ratge ($\Delta t/\Delta V$) -40°C to +85°C

 $V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$

10 ns/V

DC Electrical Characteristics

Ob.al	Parameter	Vcc	T _A = -40°	C to +85°C	Units	bus pins will be stored on every LOW-to-
Symbol		(V)	Min	Min Max		Conditions HOIH - H
V _{IH}	High Level Input Voltage	2.7-3.6	2.0		V	V _{OUT} ≤ 0.1V or
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8	1727	≥ V _{CC} - 0.1V
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	>		$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{mA}$ $I_{OH} = -18 \text{mA}$ $I_{OH} = -24 \text{mA}$
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
I _I	Input Leakage Current	2.7-3.6		±5.0	μΑ	$0 \le V_I \le 5.5V$
loz	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V (V_I = V_{IH} \text{ or } V_{IL})$
loff	Power Off Leakage Current	0		100	μΑ	$V_I \text{ or } V_O = 5.5V$
Icc	Quiescent Supply Current	2.7-3.6		10	μΑ	$V_I = V_{CC}$ or GND
			So 11	±10	μΑ	$3.6 \le (V_I, V_O) \le 5.5V$
ΔICC	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$

Symbol	Parameter	Vcc	$T_A = -40$ $C_L =$	Units	
		(V)	Min	Max (Note 2)	CAPA INT
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus	2.7 3.0-3.6	1.5 9A\115/1908	8.0 7.0 OB10	ns
t _{PHL} , t _{PLH}	Propagation Delay Clock to Bus	2.7 3.0-3.6) bnd.51uq	9.5 8.5	ns i
t _{PHL} , t _{PLH}	Propagation Delay SAB or SBA to A _n or B _n	2.7 3.0-3.6	1.5 1,5	0.5 hoas 0	I Isans o
tpzh, noitsoil tpzhona eluc	Output Enable Time	wol 10 2.7 b) m	bed for 6.httplexed retin md.5ro and bug	data direct.8 rom the in	ns nemission of
t _{PHZ} , t _{PLZ}	Output Disable Time G to A _n or B _n Am AS amia\sq	2.7 3.0-3.6	edi otni perbolo ed l -gal Hallin erit of sec ot bebiva. (ASE	approprie 2.8 Care pin c	registers. U jist en as the evol. Output
t _{PHZ} ,	Output Disable Time DIR to An or Bn	2.7 3.0–3.6	1.5 -eoilgast,5V (V8.8)	no 9.5ut teviaga	art of the tran
t _{PHZ} , t _{PLZ}	Output Disable Time DIR to An or Bn	2.7 3.0-3.6	1.5	or graceful to valid	ns with capi int an
ts	Setup Time Setup Time	2.7 3.0–3.6	grinistra.5 elidw a 2.5	a high speed operationer dissipation.	veidos ot v vos schiev
tH	Hold Time V08S < lebo	3.0-3.6	1.5 1.5		ns
tw	Pulde Width	2.7 3.0–3.6	4.0 4.0	Code: See Section	eninebr ns
toshL,	Output to Output Skew	3.0	1	alodn 1.0	ns olgo

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

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Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	T _A = 25°C	Units	Conditions
VOLP	Quiet Output Dynamic Peak VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$
V _{OLV}	Quiet Output Dynamic Valley VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

Capacitance

toslh

(Note 1)

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	Input Capacitance	96/1/9/JT 7	pF	$V_{CC} = Open$ $V_{I} = 0V \text{ or } V_{CC}$
CIVODEGE	Input/Output Capacitance	8	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
CPDKOTMS	Power Dissipation Capacitance	32	etuqiuO ®	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
200	age Maan MT	See NS Pack		F = 10 MHz



New Year not 2 notices and 180 february PRELIMINARY

74LCX652

Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

The LCX652 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

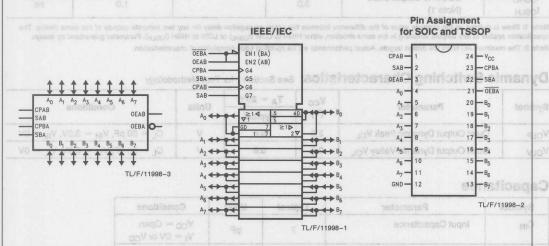
- 5V tolerant inputs and outputs
- = 11 to a language and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
 Power-down static overvoltage protection on inputs and
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 Series 652
- Latchup performance exceeds 300 mA
- ESD performance:

Human Body Model >2000V Machine/Model >250V

Ordering Code: See Section 11

Logic Symbols

Connection Diagram



Pin Names	Description
A ₀ -A ₇ , B ₀ -B ₇	A and B Inputs/TRI-STATE® Outputs
CPAB, CPBA	Clock Inputs
SAB, SBA	Select Inputs
OEAB, OEBA	Output Enable Inputs

8	SOIC JEDEC	TSSOP JEDEC
Order Number	74LCX652WM 74LCX652WMX	74LCX652MTCX
See NS Package Number	M24B	MTC24

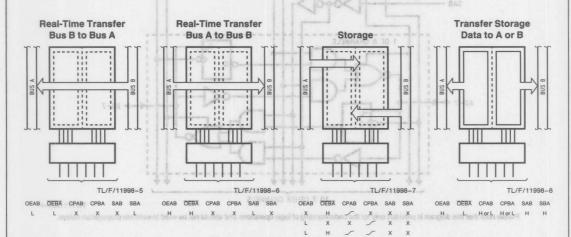
Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

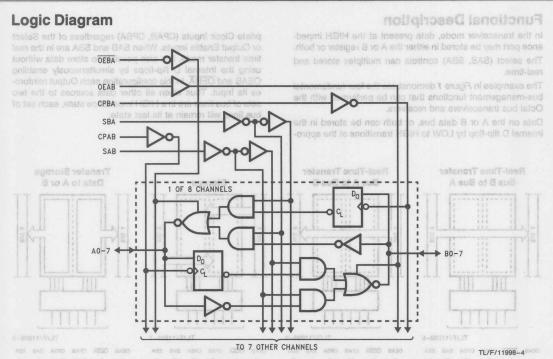
Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

priate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.



		FIGUR	E 1					
Operating Mode	Shipping					arugat		
	Bo thru By	A ₀ thru A ₇	ABS	SAIS		CPAR		
	ingut			×	J to H	J to H	н	
Store A and B Date	1000			X			Н	
Store A, Hold B	Not Specified		X	×	HorL			X
Store A in Both Registers	DulgtuC	Jugal		×			H	
Hold A, Store B		Not Specified		×	~		X	
Store B in Both Registers	input	Output				~	J	
Real-Time B Data to A Bus	tuani	fuction		×		X	1	J
			H	×	JioH	X	3	
Real-Time A Data to B Bus			×	J		X	н	
Stored A Data to B Bus		Juden		H				
Stored A Data to B Bus and Stored B Data to A Bus	Output	tuqtuO	Н		Hort			Н

Hotel The dats output functions may be enabled or disabled by vertous signals at OEAS or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HiGH transition on the clock inputs.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table (Note)

		Inpu	ts			Inputs/	Outputs	Operating Mode
OEAB	OEBA	СРАВ	СРВА	SAB	SBA	A ₀ thru A ₇	B ₀ thru B ₇	Operating mode
L	Н	HorL	HorL	X	Х	Input Input Isolation		Isolation
L	Н	_	_	X	X	mpat	mpat	Store A and B Data
×	Н	_	HorL	X	Х	Input	Not Specified	Store A, Hold B
Н	Н	5	_	X	X	Input	Output	Store A in Both Registers
L	X	HorL	_	X	X	Not Specified	Input	Hold A, Store B
L	L	_	_	X	Х	Output	Input	Store B in Both Registers
L	L	Х	Х	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	HorL	Х	Н	Cutput	Imput	Store B Data to A Bus
Н	Н	X	X	L	X	Input	Output	Real-Time A Data to B Bus
Н	Н	HorL	Х	Н	X	mpat	Cutput	Stored A Data to B Bus
Н	L	H or L	H or L	Н	н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

L = LOW Voltage Level

X = Immaterial

⁼ LOW to HIGH Clock Transition

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications

Office/Distributors for availability a	and specini	cations.
Supply Voltage (V _{CC})	-0.5V	to +7.0V
DC Input Voltage (V _I)	-0.5V	to +7.0V
Output Voltage (V _O) Outputs TRI-STATE	-0.5V -0.5V to V ₀	to +7.0V
DC Input Diode Current (I _{IK}) (V _I) < 0	1.5	-50 mA
DC Output Diode Current (I _{OK}) V _O < 0	1.6	-50 mA
Vo > Vcc	1.6	+50 mA
DC Output Source/Sink Current (IOH/	LS (Jol	\pm 50 mA
DC V _{CC} or Ground Current per Supply Pin (I _{CC} or I _{GND})	1.5	± 100 mA

Storage Temperature Range (TSTG) -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Ratings must be observed.

Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

Conditions	
Supply Voltage Operating Data Retention Only	2.0V to 3.6V 1.5V to 3.6V
Input Voltage (V _I) Output Voltage (V _O) Output in Active State	0.0V to 5.5V
Output in "OFF" State	0.0V to 5.5V
V _{CC} = 3.0V to 3.6V olsosquiq V _{CC} = 2.7V to 3.0V as 10 8.2	
Free Air Operating Temperature (T _A) Minimum Input Edge Rate (Δt/ΔV)	-40°C to +85°C
$V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$	10 ns/V

OEBA to A

DC Electrical Characteristics

Symbol	Parameter	Vcc	$T_A = -40^{\circ}C$	c to +85°C	Units	Conditions
anti anivah s	whee aril in pluratio alcusted out you in	(V)	Min	Max	av etulneris e	to be heritaly at water at a tol
V _{IH} ngleab w	High Level Input Voltage	2.7-3.6	MOJ at H2.0 reither n.	In the name direction	puts switching	1 1001 - 0.11
V _{IL}	Low Level Input Voltage	2.7-3.6	penipaga ad llay abhity	0.8	a ace design t	≥ V _{CC} - 0.1V \$ 100
Voн	High Level Output Voltage vgaloborite	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	haracteris	O cyld	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{mA}$ $I_{OH} = -18 \text{mA}$ $I_{OH} = -24 \text{mA}$
V _{OL}	Low Level Output Voltage	2.7-3.6	fayT (V)	0.2	GIBINA ISM	$I_{OL} = 100 \mu\text{A}$
V0 = _0V,	$V = 50 \text{ pF}, V_{\text{IH}} = 3.3 $	3.0	8.9 0.8	0.4	ut Dynamic	I _{OL} = 12 mA I _{OL} = 24 mA
10 = JN ,	Input Leakage Current	2.7-3.6	3.3 0.0	1±5.0 16V	μΑ	0 ≤ V ₁ ≤ 5.5V
loz	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5B$ $V_I = V_{IH} \text{ or } V_{IL}$
loff	Power Off Leakage Current	Ogjinij	Typical	100	μΑ	$V_I \text{ or } V_O = 5.5V$
lcc	Quiescent Supply Current	07.06		10	μА	$V_I = V_{CC}$ or GND
	V _I = 0V or V _{GC}	2.7-3.6	1	±10	μΑ	$3.6 \le (V_I, V_O) \le 5.5$
Δlcc	Increase in I _{CC} per Input	2.7-3.6		500	OLUAOVI	$V_{IH} = V_{CC} - 0.6V$

AC Electrical Characteristics: See Section 2 for Test Methodology 118 14 mumber 14 and 16 and

O	Parameter Spation	Con	ilred, Sales		10°C to +85°C = 50 pF	if Military/Aet please contaction
Symbol Va.8 of Va.1		(V) Open		of VaMin	Max (Note 2)	Supply Voltage
t _{PHL} ,	Propagation Delay Clock to Bus	2.7 3.0-3.6	V0.1	1.5 1.5	9.5 8.5	egatioVnsqtuC
t _{PLH}	Propagation Delay Bus to Bus	2.7 3.0-3.6	Va.0	1.5/3.0- 1.5	7.0	Ougants Activ
t _{PHL} , t _{PLH}	Propagation Delay SAB or SBA to A or B	2.7 3.0-3.6	Am 0	1.5 1.5	9.5 8.5	oold tughe Dioc
t _{PZH} 0.04 –	Output Enable Time OEBA to A	2.7 3.0-3.6	Am 0	1.5 ± 1.5 (pol	6.9 Ce/Sink (6.8 ent (I _{OH})	Vo > Voc
t _{PHZ} , t _{PLZ}	Output Disable Time OEBA to A	2.7 3.0-3.6	Am 0	1.5 1.5	9.5 muO bno (08.5 10 00f) f	DC Voc or Gro per Sn per Snupply Pi
t _{PZH} , t _{PZL}	Output Enable Time OEBA to A	2.7 3.0-3.6	150°C alues	1.5		A" edt "setok
t _{PHZ} , t _{PLZ}	Output Disable Time OEAB to B	2.7 3.0-3.6	iaran- a. The	1.5 1.5	9.5 8.5	beyond which beed and seed and
ts	Setup Time Bus to Clock	2.7 3.0-3.6	tings. fefine	2.5	sranteed at the absorded Openating Conc	g ton eins side
t _H	Hold Time Bus to Clock	2.7 3.0-3.6	ved.	1.5 1.5 m e	or actual device oper lute Maximum Pating	ne conditions in lote 2nd lote 2nd lotes
t _W	Clock Pulse Width	2.7 3.0-3.6		4.0 4.0	ical Characte	ns
toshl,	Output to Output Skew (Note 1)	3.0		ooV	1.0	ns lodiny?

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics See Section 0 for Test Methodology

Am 5	$S - = HO^{1}$	Vcc	TA = 25°C	Unite	Conditions
Symbol	por = Jol Parameter S.0	(V)	Typical	Units	V _{OL} Conditions Coulput Voltage
V _{OLP}	Quiet Output Dynamic Peak VOL	3.3	0.8	٧	$C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{V, } V_{IL} = 0 \text{V}$
Volv va	Quiet Output Dynamic Valley VOL	3.3	0.8 0.8-	V 2.	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

Capacitance

Symbol	Parameter OOT	Typical	Units	Conditions
C _{IN} 10 20 V √8.8 ≥ (6 V , V)	Input Capacitance	7	2.7-3 q q	V _{CC} = Open V _I = 0V or V _{CC}
VC(/O- 00V =	Input/Output Capacitance	8	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
C _{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$



74LCX16240

Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

General Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16240 is designed for low voltage (3.3V) $V_{\rm CC}$ applications with capacity of interfacing to a 5V signal environment.

The LCX16240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications

TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but inde-

noito PRELIMINARY

- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry

Truth Tables

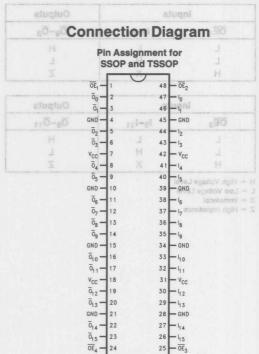
TL/F/11999-2

- Functionally compatible with the 74 series 16240
- Latchup performance exceeds 300 mA
- ESD performance:

Human body model >2500V Machine model >250V

Pin Names	Description	
OE _n I ₀ -I ₁₅ O ₀ -O ₁₅	Output Enable Inputs (Active Low) Inputs Outputs	

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16240MEA 74LCX16240MEAX	74LCX16240MTD 74LCX16240MTDX
See NS Package Number	MS48A	MTD48



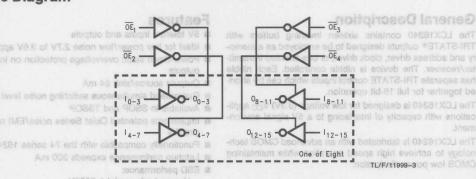
Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

TL/F/11999-1

Functional Description

The LCX16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable (OEn) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Low-Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

Truth Tables

Inputs		Outputs		
OE ₁	stori Clo-Islant	$\overline{O}_0 - \overline{O}_3$		
L	Pin Assignment for	Н		
L	SSOP HE SORE	L		
Н	X	Z		

	Inputs	1 5	Outputs	
OE ₃	45 680	I ₈ -I ₁₁	4-019	0 ₈ -0 ₁₁
L		L	3-5	Н
L	2V-122	Н	Vec = 7	L
Н	11-415	X	8 - 0	Z

Н	=	High	Voltage	Level

L = Low Voltage Level

Inp	Inputs			
OE ₂	I ₄ -I ₇ [od:	04-07		
L	L	Н		
L	Н	L		
1 1H2 1 1	X	Z		

TL/F/11999-3 00 Wol 20MO

30	Inp	Outputs	
30	OE ₄	I ₁₂ -I ₁₅	0 ₁₂ -0 ₁₅
a 10 s	0 81 210 10 010	to to to To to to to	O O O OH
101	PODD	O O OHO O O	POOPL
LIEVELE	Н	X	Z

Description	Pin Names
Output Enable Inputs (Active Low)	
Inputs Outputs	arl-ol 0-00

	SSOP EIAJ	TBSOP JEDEC
	74LCX16240MEA 74LCX16240MEAX	74LCX16240MTD 74LCX16246MTDX
See NS Package Number		MTD48

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings (Note 1) | Recommended Operating | 100 | 3 | A Conditions If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Supply Voltage Office/Distributors for availability and specifications. 2.0V to 3.6V Operating Supply Voltage (V_{CC}) -0.5V to +7.0Vr Data Retention only 1.5V to 3.6V Output Voltage (V_O) Output in Active State -0.5V to +7.0V0.0V to 5.5V DC Input Voltage (V_I) Output Voltage (Vo) Output TRI-STATE -0.5V to +7.0V0.0V to VCC Output in "OFF" State dand hugh O 0.0V to 5.5V Outputs Active (Note 2) -0.5V to V_{CC} +0.5V -50 mA Output Current IOH/IOL DC Input Diode Current (I_{IK}) V_I < 0 V_{CC} = 3.0V to 3.6V ±24 mA DC Output Diode Current (IOK) -50 mA $V_{CC} = 2.7V \text{ to } 3.0V$ ±12 mA Vo < 0 Free Air Operating Temperature (TA) -40°C to +85°C Vo > Vcc +50 mA DC Output Source/Sink Curr. (IOH/IOL) ±50 mA Minimum Input Edge Rate (Δt/ΔV) DC V_{CC} or Ground Current angles and year of value and spacetal subsection V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V per Supply Pin (I_{CC} or I_{GND}) (4,000) HORH or WCL not ±100 mAL of HORH reduce, needed as the light state of the local form of the local Note 2. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization. Storage Temperature -65°C to +150°C Range (TSTG) Note 1: The "Absolute Maximum Ratings" are those values Dynamic Switching Characteristics: beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" Symbol table are not quaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation. Note 2: In Absolute Maximum Rating must be observed. Quiet Output Dynamic Valley Vol.

DC Electrical Characteristics

Symbol	Parameter	Vcc	TA = -40°C	to +85°C	Units	Conditions
	raidinese bibbood	(V)	Min	Max	ornality.	
V _{IH}	High Level Input Voltage	2.7-3.6	2.0	8311	V	V _{OUT} ≤ 0.1V or
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8	transO trati	≥ V _{CC} - 0.1V
VoH	High Level Output Voltage VE.8 = 05V	2.7-3.6 2.7 3.0 3.0	V _{CC} -0.2 2.2 2.2	noit	werVissipal Apacitance	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -12 \text{mA}$ $I_{OH} = -18 \text{mA}$ $I_{OH} = -24 \text{mA}$
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	I _{OL} = 100 μA I _{OL} = 12 mA I _{OL} = 24 mA
կ	Input Leakage Current	2.7-3.6		±5.0	μА	$0 \le V_1 \le 5.5V$
loz	TRI-STATE Output Leakage	2.7-3.6		±5.0	μА	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$
Icc	Quietscent Supply Current	2.7-3.6		20	μΑ	V _I = V _{CC} or GND
		2., 5.0		±20	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$
loff	Power Off Leakage Current	0		100	μΑ	V_1 or $V_0 = 5.5V$

AC Electrical Characteristics: See Section 2 for test methodology Mask mumbers of pulced A

	Baramatar St. Mov. V.C.C	being rotonor Ct = 50 pF of M eth 12d nos see		
Va.C of Va.1	Parameter politice (V)	nd apacinoscons. 0, niM io +7,0V	Max (Note 2) (OOV) epatiov vique	
t _{PHL} , t _{PLH}	Propagation Delay Data to Output 2.7 3.0–3.6	1.5 1.5	5.6 4.9 (oV) gastov ns nuO	
t _{PZL} , vo. o	Output Enable Time 2.7 3.0-3.6	V3.0+ 001.5 v3.0-	7.7 sloW) ev to A sluns O 7.0	
t _{PHZ} ,	Output Disable Time of V 8 = 2.7	1.5 Am 03 — 1.5	DC entput Diode Currer7.7 Ord)	
toshi,	Output to Output 3.0	+ 50 mA + 50 mA	V No V Color Source/Sink Curr. (ICH/Ic	

Note 1. Skew is defined as the absolute value of the difference between the actual propagaton delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Note 2. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for test methodology

Cumbal	Dave service.	Vcc	T _A = 25°C	ed at these threat	read, The device should not be operate caremetric values to sed in the "Fled	
Symbol	Parameter	(V)	Typical	Units	oads and its beginning for one eldst	
V _{OLP}	Quiet Output Dynamic Peak VOL	3.3	0.8	tions V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	
V _{OLV}	Quiet Output Dynamic Valley VOL	3.3	0.8	musi V se ob	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	

DC Electrical Characteristics

Capacitance

Symbol	Paramete	r	Typical	Units	Conditions	Symbol
VOUT ≤ 0.1V or	put Capacita	nce	7 0.9	pFa.8-17.8	V _{CC} = Open V _I = 0V or V _{CC}	НΑ
THE REPORT OF THE PARTY AND THE	utput Capaci	tance	8,0-20/	PF _{3.8-7.8}	V _{CC} = 3.3V	V _{IL}
C _{PD} P	ower Dissipa apacitance	tion	32 2.2	pF 0.8 0.8	V _{CC} = 3.3V V _I = 0V or V _{CC} F = 10 MHz	
lot = 100 kA lot = 12 mA lot = 24 mA	V	0.2 0.4 0.65		2.7-3.6 2.7 3.0	Love Level Output Voltage	YoV
0 ≤ V ₁ ≤ 6.6V	Au	±5.0		2.7-3.6	Input Leakage Current	11
$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$	Ац			2.7-3.6	TRI-STATE Output Leakings	zol
VI = VCC or GND	Au	20		2.7-3.6	Quietscent Supply Current	
$3.6 \le (V_1, V_0) \le 6.6$	Au			0.0-1.0		
$V_{HH} = V_{CO} - 0.6V$	Au	500		2.7-5.6	Increase in Icc per Input	Alco
V _I or V _O = 5.5V	Au	100		0	Power Off Leakage Gurrent	lofe.



74LCX16244

getner to obtain full 16-bit operation. The TRI-STATE out-Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The 74LCX16244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate TRI-STATE control inputs which can be shorted together for full 16-bit operation.

The LCX16244 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environ-

The LCX16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications

TRI-STATE standard outputs. The device is nibble (4 bits) pendent of the other. The control plas can be shorted to-

PRELIMINARY

- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction
- Functionally compatible with the 74 series 16244
- Latch performance exceeds 300 mA
- ESD performance:

Human Body Model > 2000V Machine Model > 250V

Ordering Code: See Section 11

Logic Symbol

Connection Diagram

Pin Assignment for SSOP and TSSOP



Pin Names	Description
ŌĒ _n	Output Enable Input (Active Low)
I ₀ -I ₁₅	Inputs
00-015	Outputs

	SSOP EIAJ	TSSOP JEDEC	
Order Number	74LCX16244MEA 74LCX16244MEAX	74LCX16244MTD 74LCX16244MTD	
See NS Package Number	MS48A	MTD48	

OE	1	48	- OE ₂
00 -	2	47	- I ₀
0,-	3	46	— I ₁
GND -	4	45	- GND
02-	5	44	-12
03 -	6	43	-13
V _{CC}	7	42	- v _{cc}
04 -	8	41	-14
05 -	9	40	-1 ₅
GND -	10	39	- GND
06 -	11	38	-16
07-	12	37	- I ₇
08 —	13	36	- I ₈
09 -	14	35	— I ₉
GND —	15	34	- GND
010-	16	33	-40
011	17	32	-111
v _{cc} -	18	31	- v _{cc}
012-	19	30	-112
013-	20	29	- I ₁₃
GND -	21	28	— GND
014-	22	27	- I ₁₄
015-	23	26	- I ₁₅
OE ₄ —	24	25	$-\overline{OE}_3$

TL/F/12000-2

Functional Description

The LCX16244 contains sixteen non-inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The TRI-STATE outputs are controlled by an Output Enable (OEn) input for each nibble. When OEn is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Low-Voltage 16-Bit Buffer/Line Driver with 5V Tolerant inputs and Outputs

Truth Tables

Inputs	Outputs		
V to 3.6V 130 lostion	r/low simple?	woo wO ₀ -O ₃ ebl	
otection on inputs an	overvoltige pr	_	
L	Н	Hughuo	
Н	nk 24 mX	Outputs source/si	

/EMI reductio	Outputs	
OE ₃	I ₈ -I ₁₁	08-011
L	a exceed 300 mA	a Latch hadomany
L		ESD Herormance
Н		M vbo8 nrZnuH

In	Outputs	
OE ₂	benoteel4-l7	04-07
	ress driver, clock o	
	er. The Hevice is n	transmitter/receiv

5V signal en	Outputs	
ŌE ₄	I ₁₂ -I ₁₅	012-015
triism eLdw	high speed operation	nolock to achieve
L	dissipat H n.	CMCH low power
Н	X	Z

Ordering Code: See Section 11

Connection Diagram Pin Assignment for

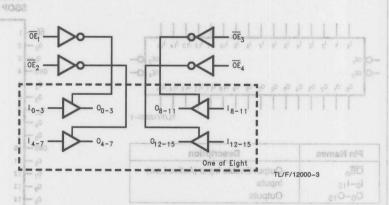


47 -10

37 -17

36 1-10 34 - GND

30 --- 12



	SSOP EIAJ	TSSOP JEDEC
Order Number	74LCX16244MEA 74LCX16244MEAX	Z4LCX16244MTD Z4LCX16244MTDX
See NS Package Number	MS48A	MTD48

H = High Voltage Level

L = Low Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Ratings (Note 1) 101 5 10

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Office/ Distributors for availability	and specifications.
Supply Voltage (VCC)	-0.5V to $+7.0V$
DC Input Voltage (V _I)	-0.5V to $+7.0$ V
Output Voltage (V _O)	
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5 V to $V_{CC} + 0.5$ V
DC Input Diode Current (I _{IK}) V _I < 0	-50 mA
DC Output Diode Current (IOK)	
V _O < 0	-50 mA
Vo > Vcc	+50 mA
DC Output Source/Sink Current (IOH	/I _{OL}) ±50 mA
001/	

DC V_{CC} or Ground Current
per Supply Pin (I_{CC} or I_{GND}) ± 100 mA
Storage Temperature Range (TSTG) -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Io Absolute Maximum Rating must be observed.

Recommended Operating A

Gollandono	
Supply Voltage Operating Data Retention Only	2.7V to 3.6V 1.5V to 3.6V
Input Voltage (V _I)	0V to 5.5V
Output Voltage (Vo)	
Output in Active State Output in "OFF" State	0V to V _{CC} 0V to 5.5V
Output Current I_{OH}/I_{OL} $V_{CC} = 3.0V$ to $3.6V$ $V_{CC} = 2.7V$ to $3.0V$	±24 mA ±12 mA
Free Air Operating Temperature (TA)	-40°C to +85°C
Minimum Input Edge Ratge (Δt/ΔV)	низот
$V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$	10 ns/V

DC Electrical Characteristics

Symbol	Povemeter	Vcc	$T_A = -40^{\circ}C$	to +85°C	Units	Conditions	
Syllibol	Parameter	(V)	Min Max		Units	Conditions	
VIH	High Level Input Voltage	2.7-3.6	2.0	1035	V	V _{OUT} ≤ 0.1V or	
V _{IL}	Low Level Input Voltage	2.7-3.6	A DESCRIPTION	0.8	Capacitaros	≥ V _{CC} - 0.1V	
V _{OH}	High Level Output Voltage V	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	90	ut C y acitan	$I_{OH} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OH} = -18 mA$ $I_{OH} = -24 mA$	
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0	32	0.2 0.4 0.55	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	
lį	Input Leakage Current	2.7-3.6		±5.0	μΑ	$0 \le V_I \le 5.5V$	
loz	TRI-STATE Output Leakage	2.7-3.6		±5.0	μА	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$	
loff	Power Off Leakage Current	0		100	μΑ	$V_I \text{ or } V_O = 5.5V$	
lcc	Quiescent Supply Current	2.7-3.6		20	μΑ	$V_I = V_{CC}$ or GND	
		2.7-0.0		±20	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$	
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$	

AC Electrical Characteristics: See Section 2 for Test Methodology 1889 munities 4 studes da

Symbol	Parameter Parameter	T _A = -40° C _L =	Units	
2.7V to 3.6V Va 8 ot Va 1	(V) perating	V0.5+ 0/Ming-	Max (Note 2)	Supply Voltag
VªPHL VO tPHL	Propagation Delay (V) eg 510V 12.7	V0.7 + of 1.5.0 - 1.5	5.2 (oV) e	DC Input Voit en Output Voltar
t _{PZL} VO	Output Enable Time 2.7	V0.7+ of 1.50- V0.0+ oct v0.0-	7.7 STATE-1 7.0 Stole St	Outputs TR
A tPHZ	Output Disable Time 2.7 2.7 3.0-3.6	1.5 Am 08 – 1.5	(xo) 7.7 mu3 ebo	O samput D
toshi,	Output to Output Skew 3.0 (Note 1) (Note 1)	+50 mA lou) ±50 mA	urce/Sink@trrent (lon	OC Surput Sc

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaran-

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	T _A = 25°C	Units on	table are not guaranteed at the absolute 'The 'Reco enolitions conditions' or the conditions are the conditions and device are the conditions are the conditions.
V _{OLP}	Quiet Output Dynamic Peak VOL	3.3	0.850008	musVbe of	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$
V _{OLV}	Quiet Output Dynamic Valley VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

annilliana?	and the last	C to +85°C	$r_{A} = -40$	Vec		
Capacitance	sinu	mals	relité	(V)	Parameter	Symbol
Symbol 2 TUOV	Param	eter	Typical	Units	Conditions and eval note	
C _{IN} Inpu	t Capacitano	ce 8.0	7	2.7-3.6	V _{CC} = Open han level woll	71/
I _{OH} = -100 µA			Voc - 0.2	PF 9.7-3.6	V _I = 0V or V _{CC} O evel doll	но\
Cout Si - HOutp	out Capacitar	nce	2.2	pF _{0.6}	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$	
C _{PD} Pow	er Dissipatio	on Capacitance	2.2	3.0	V _{CC} = 3.3V	
$l_{OL} = 100 \mu A$ $l_{OL} = 12 mA$	V	0.2	32	PF-7.2	V _I = 0V or V _{CC} F = 10 MHz	
IOL = 24 mA		0.55		3.0		
	Aaq	±5.0		2.7-3.6	Input Leakage Current	
$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$	Ası	±5.0		2.7-3.6	TRI-STATE Output Leakage	ZC
$V_{\rm J} \text{or} V_{\rm O} = 5.5 \text{V}$	Au	100			Power Off Leakage Current	390
VI = VOC or GND	Ащ	08		2.7-3.6	Quiescent Supply Current	
3.6 ≤ (V _L , V _O) ≤ 5.5	Au	08 ±				
$V_{OC} - 0.6V = HIV$	Au	500		2.7-3.6	Increase in Ico per Input	001



PRELIMINARY

74LCX16245

Low-Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The 74LCX16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE® outputs and is intended for bus oriented applications. The device is designed for low voltage (3.3V) $V_{\rm CC}$ applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The ${\rm T/R}$ inputs determine the direction of data flow through the device. The $\overline{\rm OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

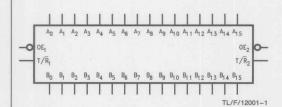
Bus Bo-By Data to Bus Ag-Ay

- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Separate control logic for each 8-bit
- Guaranteed simultaneous switching noise level
- Available in SSOP, TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with 74 series 16245
- Latchup performance exceeds 300 mA
- ESD performance:

Human body model >2000V Machine model >250V

Ordering Code: See Section 11

Logic Symbol



Pin Names	Description
ŌĒ	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs or TRI-STATE Outputs
B ₀ -B ₁₅	Side B Inputs or TRI-STATE Outputs

	SSOP EIAJ	TSSOP JEDEC		
Order Number	74LCX16245MEA 74LCX16245MEAX	74LCX16245MTD 74LCX16245MTDX		
See NS Package Number	MS48A	MTD48		

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12001-2

Truth Tables

Inputs OE ₁ T/R ₁		Outputs		
L	Н	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇		
Н	X	HIGH Z State on A ₀ -A ₇ , B ₀ -B ₇		

Inputs		Outputs
OE ₂	T/R ₂	January and Outputs
L	L	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅
L	H	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅
H	X	HIGH Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅

with 5V Tolerant Inputs and Outputs

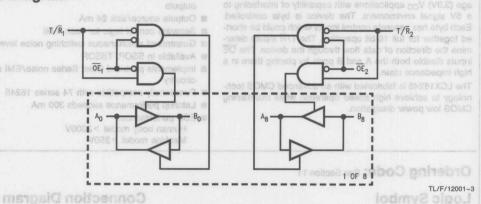
Incohold FEE

- H = High Voltage Level
- L = Low Voltage Level
- X = Immaterial
- Z = High Impedance

tdeat for low power/low noise 2.7V to 3.6V applications # Power-down static overvoise marganal

33 - A10

81 - 018



Pin Assignment for SSOP and TSSOP

| SSOP and TSSOP | Assignment for Assignment f

Pin
Names

Pares

Output Enable input

T/R

Transmit/Receive input

Ao-Ars

Side A Inputs or TRI-STATE Outputs

 SSOP EIAJ
 TSSOP LEDEC

 Order Number
 74LCX16245MEA
 74LCX16245MTD

 74LCX16245MEAX
 74LCX16245MTDX

 See NS Package
 MS46A
 MTD48

 Number
 MS6A
 MTD48

Symbol

Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage (VCC) -0.5V to +7.0VDC Input Voltage (V_I) -0.5V to +7.0VOutput Voltage (Vo) Outputs TRI-STATE -0.5V to +7.0VOutputs Active (Note 2) -0.5V to $V_{CC} + 0.5$ V -50 mA DC Input Diode Current (IIK) (VI) < 0 DC Output Diode Current (IOK) -50 mA Vo < 0 a. + 50 mA Vo > Vcc DC Output Source/Sink Current ±50 mA (IOH/IOL)

DC V_{CC} or Ground Current per Supply Pin (ICC or IGND)

±100 mA Storage Temperature Range (TSTG) 65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The page 1801 to 1818 parametric values defined in the "Electrical Characteristics" table are not quaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: In Absolute Maximum Rating must be observed.

2.0V to 3.6V 1.5V to 3.6V
0.0V to 5.5V
0.0V to V _{CC}
0.0V to 5.5V
HZQ1
teH2;
-40°C to +85°C
10 ns/V

Parameter

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions
	raiameter		Min	Max	Offics	Conditions
VIH	High Level Input Voltage	2.7-3.6	2.0	103011	out CV paci	V _{OUT} ≤ 0.1V or
VIL	Low Level Input Voltage	2.7-3.6	7	0.8		≥ V _{CC} - 0.1V
VoH	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} -0.2 2.2 2.4 2.2	Capacitance	out/Output V wer Dissip	$I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0	30	0.2 0.4 0.55	٧	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
lı	Input Leakage Current @ OE, T/R	2.7-3.6		±5.0	μΑ	$0 \le V_I \le 5.5V$
loz	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$
IOFF	Power Off Leakage Current	0		100	μΑ	$V_I \text{ or } V_O = 5.5V$
I _{CC} Quietscent Supply	Quietscent Supply Current	2.7-3.6		20	μΑ	$V_I = V_{CC}$ or GND
		2 0.0		±20	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$

AC Electrical Characteristics: See Section 2 for Test Methodology 1657 (1997) AC Electrical Characteristics: See Section 2 for Test Methodology 1657 (1997) AC Electrical Characteristics: See Section 2 for Test Methodology

O	Conditions	TA = +40	0°C to +85° 53808314 A\vishid ti
Va.Symbols Va.S of Va.1	Parameter (V)	V0.7 + 01Min 0 - 0.0V	Max (Note 2)
t _{PHL} ,	Propagation Delay 2.7 Clock to Bus 3.0-3.6	1.5 /0.7 + of 1.50 -	5.8 (oV) a saloV instruo 5.2 ETATE-LIT supplied
t _{PZL} ,	Output Enable Time 2.7 OEBA to A 3.0-3.6	78.0 + 001.51 V8.0 - Am 08 - 1.5	0 > ((V) (7.2 Normal Dioce Current 2.7)
t _{PHZ} ,	Output Disable Time 2.7 OEBA to A 3.0-3.6	1.5 Am 08 + 1.5	8.0 7.2
toshl,	Output to Output Skew (Note 1) 3.0	Am 08 ±	DC Output Source/Sink Current (ISA/Iot) 0.1

Note 1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Note 1: The "Absolute Maximum Ratings" are those values

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	Vcc	T _A = 25°C	Units	veds ent to become to ton ene eldet	
Зушьог	raiametei	(V)	Typical	and of the same	The "Recognitions for actual device apart	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	0.8	musVbe oi	$C_{L} = 50 \text{ pF, V}_{IH} = 3.3 \text{V, V}_{IL} = 0 \text{V}$	
V _{OLV}	Quiet Output Dynamic Valley VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	

apacitano	ce	uninu	0 to +86°C	704 - = AT	VCC (V)	Paramoter	Symbol
Symbol	17	Parar	meter	Typical	Units	Conditions	
C _{IN}	Input	Capacit	tance 8.0	7	8.8 PFs	V _{CC} = Open V _I = 0V or V _{CC}	HI/
C1/0	Input	/Output	Capacitance	V ₈ -0.2	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$	но
C _{PD}		r Dissip	ation	2.2	0.0	V _{CC} = 3.3V	
	Capa	citance	\$.0	32	9.8-7.S	$V_I = 0V \text{ or } V_{CC}$ F = 10 MHz	
= 24 mA	ioi l	4	0.65		0.6		
< V ₁ ≤ 5.5V	0		±5.0		2.7-3.6	Input Leakage Current @ ČE, T/R	
		Ац	±5.0		2.7-3.6	TRI-STATE I/O Leslæge	30
or Vo = 5.5V	IA	Au	100			Power Off Leakage Current	
= V _{CC} or GND		Au	OS 20		2.7-3.6	Quietscent Supply Current	
$\delta \leq (V_1, V_0) \leq 5.5$		Ац	0S±				
V8.0 - 0.6V = H	W.V		800			Increase in Ioc per input	

74LCX16373

Low-Voltage 16-Bit Transparent Latch (6.3.) elden 3 rotal ent north shed with 5V Tolerant Inputs and Outputs transparent, i.e. a latch output will change

General Description

See NS Package

Number

MS48A

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z

The LCX16373 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environ-

The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features in 0 ent no tresero sew tent notemorni

- 5V tolerant inputs and outputs | 5H out on boosing
- Ideal for low power/low noise 2.7V to 3.6V applications

The LCX16373 contains styteen D-type latches with

the other. Control pins can be shorted together to obtain full

notiginos PRELIMINARY

- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16373
- Latchup performance exceeds 300 mA
- ESD performance:

Human Body Model > 2000V Machine Model > 250V

Ordering Code: See Section 11 **Logic Symbol Conection Diagram** Pin Assignment for SSOP and TSSOP 48 40 41 42 43 44 45 47 00 OE, 0, -LE GND . 45 - GND 02 03 -43 42 TL/F/12002-1 Vcc 41 0, 05 40 39 GND -- GND 06 -38 **Pin Names** Description 12 37 07 -0E_n Output Enable Input (Active Low) 36 08 -13 LEn Latch Enable Input 35 09 -10-115 Inputs 15 34 GND -- GND Outputs 00-015 010 33 32 011-18 31 VCC . - Vcc 19 30 012 -1/12 SSOP EIAJ **TSSOP JEDEC** 20 29 013--113 GND -21 28 - GND Order Number 74LCX16373MEA 74LCX16373MTD 22 27 0,4 74LCX16373MEAX 74LCX16373MTDX 23 015 26 -45

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

OE2 -24 25 - LE2

MTD48

Functional Description

The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LEn) input is HIGH, data on the Dn enters the latches. In this condition the latches are transparent, i.e. a latch output will change states each time its D input changes. When LEn is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LEn. The TRI-STATE standard outputs are controlled by the Output Enable (OEn) input. When OEn is LOW, the standard outputs are in the 2-state mode. When OEn is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

m Implements patented Quiet Series noise/EMI reduction

Functionally compatible with the 74 series 16373

■ Latchup performance exceeds 300 mA

Truth Tables

	Inputs					
LE ₁	OE ₁	10-17	00-07			
X	Н	X	Z			
Harry &	ig Lar	anottal	Varior 1			
Hana	Sen Fer I	A COH IN	H			
s afua	rank in	SOX V	00			

	Inputs Grand			
LE ₂	OE ₂	I ₈ -I ₁₅	O ₈ -O ₁₅	
		devicX is byte		
		to the gata when low, ghe data		
the Oytput	he bus when	a appyars on the	oo beroo	

H = High Voltage Level

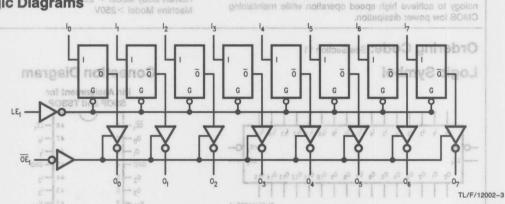
L = Low Voltage Level The LCX16373 is designed for low v

X = Immaterial on the capability of interfacing papers with capability and the capability of interfacing and another capability of the capability of the

O₀ = Previous O₀ before HIGH to LOW transition of Latch Enable

The LCX16373 is fabricated with an advanced CMOS tech-

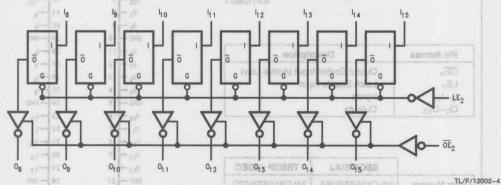
Logic Diagrams



ai en

circuitry

ESD performance:



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Voltage (V _I)	-0.5V to +7.0V
Output Voltage (V _O) Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to V _{CC} +0.5V
DC Input Diode Current (I _{IK}) V _I < 0	-50 mA
DC Output Diode Current (IOK)	1.6
V ₀ < 0	-50 mA
Vo > Vcc	+ 50 mA
DC Output Source/Sink Current	
(IOH/IOL)	±50 mA
DC V _{CC} or Ground Current	
per Supply Pin (I _{CC} or I _{GND})	±100 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

Supply Voltage Operating Data Retention Only	2.0V to 3.6V 1.5V to 3.6V
Input Voltage (V _I) Output Voltage (V _O) Output in Active State	0.0V to 5.5V
Output in "OFF" State Output Current I _{OH} /I _{OL} V _{CC} = 3.0V to 3.6V V _{CC} = 2.7V to 3.0V	± 24 mA ± 12 mA
Free Air Operating Temperature (T_A) Minimum Input Edge Rate ($\Delta t/\Delta V$) $V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	-40°C to +85°C
	H ²

DC Electrical Characteristics

Symbol	Parameter	V _{CC} T _A = -		C to	+85°C	Units	Conditions	
Symbol	raidilletei	(V)	as Min	dov	Max	Oille	- Conditions	
VIH	High Level Input Voltage	2.7-3.6	2.0	(V)		V	V _{OUT} ≤ 0.1V or	
VID - V	Low Level Input Voltage	2.7-3.6	8.0	3.0	0.8	mic Pask	≥ V _{CC} - 0.1V	
Voн	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	0.8	,oV1	ellsV oim V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0	ezinU ls	siqy'	0.2 0.4 0.55	V	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{mA}$ $I_{OL} = 24 \text{mA}$	
l _l	Input Leakage Current	2.7-3.6	Pq pF	1	±5.0	μΑ	0 ≤ V _I ≤ 5.5V	
loz	TRI-STATE Output Leakage	2.7-3.6			±5.0	μΑ	$0 \le V_O \le 5.5V$, $V_I = V_{IH}$ or V_{IL}	
loff	Power Off Leakage Current	V. 0	-lg	8	100	μΑ	V_{I} or $V_{O} = 5.5V$	
Icc	Quiescent Supply Current	2.7-3.6			20	μΑ	V _I = V _{CC} or GND	
	20 V 10 V0 =	V 2	Rq	32	±20	μΑ 👓	$3.6 \le (V_I, V_O) \le 5.5V$	
Δlcc	Increase in I _{CC} per Input	2.7-3.6		-	500	μΑ	$V_{IH} = V_{CC} - 0.6V$	

AC Electrical Characteristics: See Section 2 for Test Methodology

Cumbal	Parameter	Aldding Acc	sales dales		0°C to +85°C = 50 pF	n Military/Assi Diease contai Units Units
Va. Symbol Va. o 1 Va. r	Retention Only	(v) Open	7.0V	of Value	Max (Note 2)	Supply Voltage
t _{PHL} ,	Propagation Delay Data to Output	2.7 3.0-3.6	7.0V	1.5 0 V 1.5	7.7 7.0 (OV)	egatloVnsqtuO
tPLH	Propagation Delay LE to Output	2.7 3.0-3.6	O.SV O mA	+ 00V 1.5/8.0 - 8 - 1.5	e (Note 27.7 Current (0.7) < 0	Outputs Activ 20 DC Input Diode
Am tpZH,	Output Enable Time V0.8 = V0.8 of V7.9 =	2.7 30 3.0-3.6	Am 0	1.5 1.5	(ж28,0 петиО е 7.2	DO Output Diod 80 V
t _{PHZ} , 004-	n Input Edge Rate (At/AV)	2.7 3.0-3.6	Am 0	1.5 1.5	8.0 ce/Sink <u>9.7</u> rent	PC Conput Sou
V\ats	Setup Time V0.3 of V8.0	2.7 3.0-3.6	Amo	2.5 2.5		CIONHOI)
t _H	Hold Time	2.7 3.0-3.6	20°03	+ 01 1.5	alure Range (Tare)	Storen Tempe
t _W	Clock Pulse Width	2.7 3.0-3.6	arono aran- The	4.0	he safety of the devi schould not be opera	110
toshl, toshh	Output to Output Skew (Note 1)	3.0	stics" fings,	sincal Character. Iule masimum ra	ss defined in the "Ele aranteed". the absu	parametric valu table are not gr

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

DC Electrical Characteristics

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	Vcc	T _A = 25°C	Units	Conditions
Cymbol	VOUT ≤ 0.1V or	(V)	Typical	27-3	V _{IH} High Level input Voltage
VOLP	Quiet Output Dynamic Peak VOL	3.3	0.8	V-7-V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$
V _{OLV}	Quiet Output Dynamic Valley VOL	3.3	0.8	V	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V

Capacitance

Am 81 - = HO

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	Input Capacitance).8± 7	pF 3.8	$V_{CC} = Open$ $V_{I} = OV \text{ or } V_{CC}$
C _{OUT} V.V	Output Capacitance	8 100	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
OHD QH2 V3.8 ≥ (Power Dissipation Capacitance	0S 0S± 32	pF 8.8	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$

74LCX16374 Low-Voltage 16-Bit D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

See NS Package Number

The LCX16374 contains sixteen non-inverting D flip-flops with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (CE) are common to each byte and can be shorted together for full 16-bit operation.

The LCX16374 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs ave ene adolt-gill ent to
- Ideal for low power/low noise 2.7V to 3.6V applications

state of their individual D inputs that

The device is byte controlled with each byte functioning

- Power-down static overvoltage protection on input and output
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry

015 - 23

OE₂ - 24

- Functionally compatible with the 74 series 16374
- Latchup performance exceeds 300 mA
- ESD performance:

Human Body Model > 2000V Stage Colored Machine Model > 250V

Ordering Code: See Section 11 **Connection Diagram Logic Symbol** Pin Assignment for SSOP and TSSOP OE, - CP. 41 42 43 44 45 00 47 -10 0, 46 OF. GND - GND 0, 02 03 04 05 06 07 08 09 010 011 012 013 014 015 03 43 42 TL/F/12003-1 04 05 GND . 39 - GND Pin 38 Description **Names** 12 37 07 -17 36 13 0E_n Output Enable Input (Active Low) 09 35 CPn Clock Pulse Input GND -15 34 - GND Inputs 10-115 0,0 16 33 Outputs 00-015 32 31 19 30 012 0.21420 - I₁₃ 013 20 SSOP EIAJ **TSSOP JEDEC** 28 - GND GND 27 - 114 Order Number 74LCX16374MEA 74LCX16374MTD

TL/F/12003-2
Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

74LCX16374MTDX

MTD48

74LCX16374MEAX

MS48A

-115

26

25 - CP2

Functional Description

The LCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CPn) transition. With the Output Enable $(\overline{\sf OE}_n)$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{\sf OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the ${\sf OE}_n$ input does not affect the state of the flip-flops.

■ Guaranteed simultaneous switching noise level

≅ Functionally competible with the 74 series 16374 ■ Latchup performance exceeds 300 mA.

m Implements patented Quiet Series noise/EMI reduction

M Available in SSOP and TSSOP

m ESD performance:

Truth Tables

	Inputs				
CP ₁	OE ₁	I ₀ -I ₇	00-07		
_	L	(16874	THILC!		
1150	ristar	ep Lio	L 00		
X	Harris Harris	X	Z		

	Inputs	1 Descript	Outputs
CP ₂	OE ₂	a en la-l15 478	08-015
	nd is intende		WITH THI-ST
/		. The device is b	applications
	are common full 10-bit op	tiput Enable (CE	O bris (50)
	do madi no	int tarriding not	INTERNATION INTO IN

H = High Voltage Level

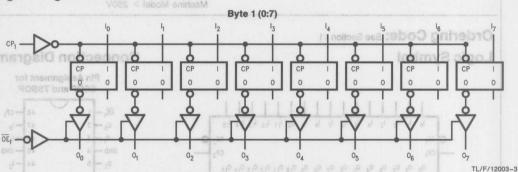
L = Low Voltage Level

X = Immaterial

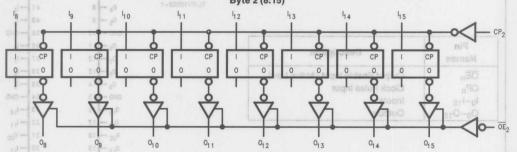
1001 Z = High Impedance

DOM: O0 = Previous O0 before HIGH to LOW of CP

Logic Diagrams S < lebol your nomes



Byte 2 (8:15)



TL/F/12003-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

 Order Number
 7ALCX16374MEA
 7ALCX16374MEA
 7ALCX16374MED
 0,4 — 22
 22
 27 — 1,4

 See NS Package Number
 MS48A
 MTD48
 00,2 — 24
 25 — 02,2
 24 — 25 — 02,2
 25 — 02,2
 25 — 02,2
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 25 — 02,2

Absolute Maximum Ratings (Note 1) and Recommended Operating 10-013 OA

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

Office/Distributors for availability	and specifications.
Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Voltage (V _I)	-0.5V to +7.0V
OutputVoltage (Vo)	1.5
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	$-0.5V$ to $V_{CC} + 0.5V$
DC Input Diode Current (I _{IK})	G.I
V _L < 0 0.8	ē. t −50 mA
DC Output Diode Current (IOK)	1.5
V _O < 0	-50 mA
Vo > Vcc	+50 mA
DC Output Source/Sink Current (IOH/	(IOL) +50 mA
DC V _{CC} or Ground Current	1.5
per Supply Pin (I _{CC} or I _{GND})	± 100 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Note 1: The "Absolute Maximum Rate	ings" are those values
beyond which the safety of the devi teed. The device should not be opera parametric values defined in the "Ele-	ted at these limits. The

the conditions for actual device operation, reliably non-negative specifical was a stage of the second sta Note 2: IO Absolute Maximum Rating must be observed.

Conditio	ns	
Supply Voltage Operating Data Retent	e (V _{CC})	2.0V to 3.6V 1.5V to 3.6V
Input Voltage	Propagation Delay (IV)	0.0V to 5.5V
Output Voltage	CP to Output (oV) e	HJQJ
Output in Ac	otive State	0.0V to V _{CC} 0.0V to 5.5V
Output Curren V _{CC} = 3.0V V _{CC} = 2.7V	to 3.6V eldseld lughuO	±24 mA ±12 mA
	ating Temperature (T _A)	-40°C to +85°C
Minimum Inpu $V_{IN} = 0.8V$	t Edge Rate ($\Delta t/\Delta V$) to 2.0V, $V_{CC} = 3.0V$	10 ns/V
2.7	Pulse Width	W ³
3.0	Output to Output Sleew (Note 1)	Toshu

Dynamic Switching Characteristics: See Section 2 for Test Methodology DC Electrical Characteristics

Cumbal	Parameter	Vcc las	TA = +40°	Units	Symbol	
Symbol VO = JIV	V C _L = 50 pF, V _{IH} = 3.3V	(V) 8	o Min 8.8	Max		Conditions UO teluO 9UOV
VIH= IV.	High Level Input Voltage	2.7-3.6	2.0	c Valley Vol.	out Cynam	V _{OUT} ≤ 0.1V or
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8	V	≥ V _{CC} - 0.1V
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	refer	V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OH} = -18 mA$ $I_{OH} = -24 mA$
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0	7	0.2 0.4 0.55	Capacitan V ut Capacita	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{mA}$
l _l	Input Leakage Curent	2.7-3.6	8	±5.0	μА	0 ≤ V ₁ ≤ 5.5V
loz	TRI-STATE Output Leakage	2.7-3.6	32	±5.0	μA	$0 \le V_O \le 5.5V$ $V_L = V_{IH} \text{ or } V_{IL}$
IOFF	Power Off Leakage Current	0	IL	100	μА	$V_1 \text{ or } V_0 = 5.5V$
lcc	Quiescent Supply Current	2.7-3.6		20 ±20	μΑ	$V_{I} = V_{CC} \text{ or GND}$ 3.6 \le (V _I , V _O) \le 5.5V
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$

table are not guaranteed at the absolute maximum ratings. and newlest entering and to enter entering and the absolute maximum ratings. The "Recommended Operating Conditions" table will define at Holls units noticelly entire studies and regarded enti

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter (SOV) 998	Vcc (V)	seles notification CL	noo eeelq	
2.6V to 3.6V 1.5V to 3.6V	viaO noito	Contractor contractor	-0. niM o +7.0V	Max (Note 2)	Supply Voltag
t _{PLH}	Propagation Delay CP to Output	3.0-3.6	V0.7 + 09\5\0- 1.5	7.7 (IV) egg 7.0 (oV) e	DC Input Volt output Voltage
t _{PZH} ,	Output Enable Time	2.7 3.0-3.6	V0.V + 61 V0.0 - V0.S + 61 V0.S + 61 V0.0 - V0.S + 61 V0.S	0.0	Outpurs 18 Canouts Ac
AntPHZ.	Output Disable Time	2.7 3.0-3.6	Am 08— 1.5 1.5	8.0 (xio17.2emi) ebo	V < 0 en DC Output D
0°48+ of 0°04-	Setup Time agment grids out Edge Rate (AVAV)		Am 08 - 2.5 Am 08 + 2.5	P. 4. 40 1 100	0 > 0V 00V <nsv< td=""></nsv<>
tH	Hold Time	2.7 3.0-3.6	1.5 Am 007 1.5	ound Current Pin (Inc or lawn)	
t _W	Pulse Width	2.7 3.0-3.6	- 05°03! + 150°00 ngs" ara 0.4se values	serature Range (Tsrg) Absolute Maximum Rat	ns
T _{OSHL} , T _{OSLH}	Output to Output Skew (Note 1)	3.0	ed at these limits. The	the salety of the devi ice should 0.h t be opera- tuce defined in the "Fla-	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two seperate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

Note 2. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Note 2: In Absolute Maximum Rating must be observed.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Cumbal	Paramatar	Vcc	T _A = 25°C	sonar	DC Electrical Character	
Symbol	Parameter 3°88+ or	ু.(V) =	AT Typical ap	Units	Conditions	
V _{OLP}	Quiet Output Dynamic Peak VOL	3.3	0.8 (W)	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	
V _{OLV} V	Quiet Output Dynamic Valley VOL	3. 0.	0.8 8.8	SV	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	

Capacitance

			110					oapaoitai
		Conditions	Units	Typical	eter	Parame	HO	Symbol
10V	. Low Leve	V _{CC} = Open V _I = 0V or V _{CC}	2.7 Aq6	7	0.2	Capacitance	Input	C _{INAU} gor
		V _{CC} = 3.3V	pF	8	ice 88.0	ut Capacitan	Outpu	Cout
	InputLea		27.38		0.84	Ass		V23>,
loz	TRI-STAT	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$	2.7 Aq 8	32	Capacitance	er Dissipation	Power	C _{PD} 2 2 0
IOFF	Power Of	Leakage Carrent	0		901	Au	70 IV	ve.c = ov
loc	Quiescen	t Supply Current	2.7-3.6		20 ±20	Aug		V_{CC} or GND: $(V_1, V_Q) \le 5.5$
Alco		in loc per Input	2.7-3.8			Au		

PRELIMINARY



74LCX16646

Low-Voltage 16-Bit Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16646 contains sixteen non-inverting bidirectional registered bus transceivers with TRI-STATE® outputs, providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition. The four fundamental handling functions available are illustrated in Figure 1 thru Figure 4.

The LCX16646 is designed for low voltage (3.3V) $V_{\rm CC}$ applications with capability of interfacing to a 5V signal environment

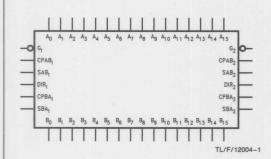
The LCX16646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16646
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human Body Model < 2000V Machine Model < 250V

Ordering Code: See Section 11

Logic Symbol



	SSOP EIAJ	TSSOP JEDEC	
Order Number	74LCX16646MEA 74LCX16646MEAX	74LCX16646MTD 74LCX16646MTDX	
See NS Package Number	MS56A	MTD56	

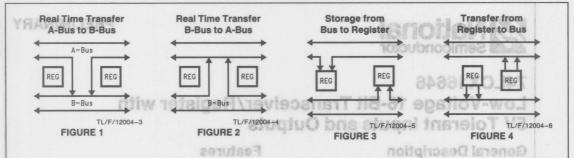
Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12004-2



The LCX18646 contains sixteen non-inverting bidirectional

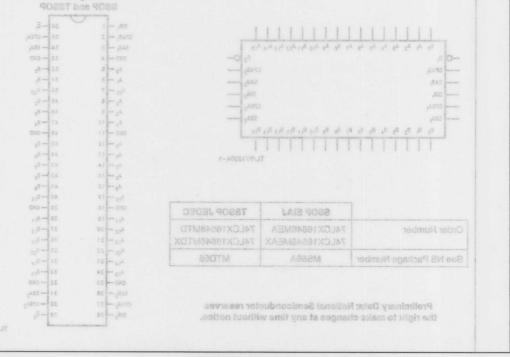
registered bus transceivers with TRI-STATE® outputs, pro-

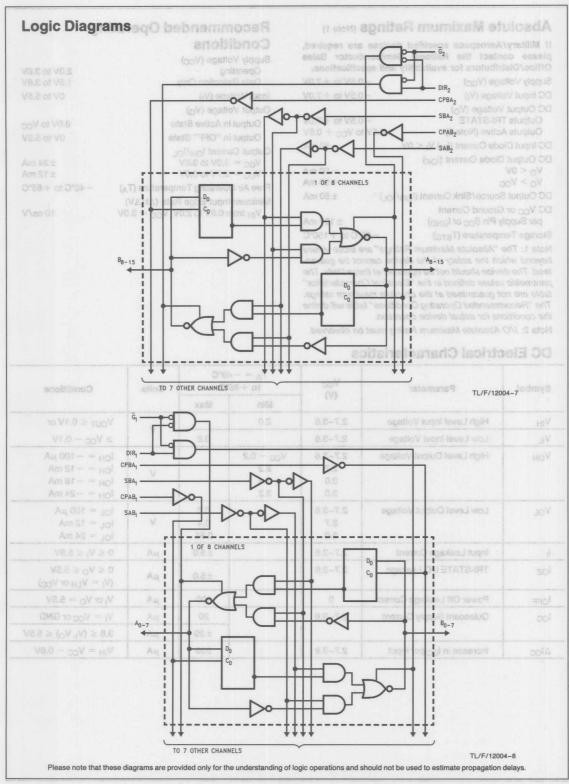
Function Table (etc/) (etc/) Edeal for low power/is (etc/) (etc/)

Power-down static overvolisace protection on inputs and cultinuts				Power-d	Data	1/0	Output Operation Mode	
G ₁	DIR ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA1	A ₀₋₇	B ₀₋₇	separate control inputs which can be she
H H NAido	X X EMXredu		H or L		ideligvA 1	atuqni Input har	and CPBA and CPBA Hugnlyst wallable ar	Isolation Clock An Data into A Register Clock Bn Data Into B Register
	H H H	H or L	atibleXwith to	perturna for Hance	LeXtrup	Input ive	OUTPUT VE	An to Bn—Real Time (Transparent Mode) Clock An Data to A Register A Register to Bn (Stored Mode) Clock An Data into A Register and Output to Bn
L	L L L	X X X	X S HorL	X X X X	H H	Output	nism elidw Input	Bn to An—Real Time (Transparent Mode) Clock Bn Data into B Register B Register to An (Stored Mode) Clock Bn into B Register and Output to An

Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level X = Immaterial





Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) -0.5V to +7.0V DC Input Voltage (V_{I}) -0.5V to +7.0V DC Output Voltage (V_{O})

Outputs TRI-STATE -0.5V to +7.0V Outputs Active (Note 2) -0.5V to $V_{CC} + 0.5V$ DC Input Diode Current (I_{IK}) $V_{I} < 0V$ -50 mA

DC Output Diode Current (I_{OK})

 $V_{\rm O} < 0V$ —50 mA $V_{\rm O} > V_{\rm CC}$ DC Output Source/Sink Current ($I_{\rm OH}/I_{\rm OL}$) \pm 50 mA

DC V_{CC} or Ground Current

per Supply Pin (I_{CC} or I_{GND}) ± 100 mA Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I/O Absolute Maximum Rating must be observed.

Recommended Operating and algolic Conditions

Supply Voltage (V_{CC})
Operating

 Operating
 2.0V to 3.6V

 Data Retention Only
 1.5V to 3.6V

 Input Voltage (V_I)
 0V to 5.5V

Output Voltage (Vo)

Output in Active State 0.0V to V_{CC}
Output in "OFF" State 0V to 5.5V

Output Current IOH/IOL

 $V_{CC} = 3.0V \text{ to } 3.6V$ $\pm 24 \text{ mA}$ $V_{CC} = 2.7V \text{ to } 3.0V$ $\pm 12 \text{ mA}$

Free Air Operating Temperature (T_A)

Minimum Input Edge Rate ($\Delta t/\Delta V$) V_{IN} from 0.8V to 2.0V, $V_{CC}=3.0V$ 10 ns/V

-40°C to +85°C

DC Electrical Characteristics

Symbol	Parameter	Vcc	$T_A = -4$ to +85		Units	Conditions	
1-60	TLIFFIZE	(V)	Min Max			Conditions	
V _{IH}	High Level Input Voltage	2.7-3.6	2.0	-	D-V	$V_{OUT} \le 0.1V$ or	
V _{IL}	Low Level Input Voltage	2.7-3.6		0.8		\geq V _{CC} $-$ 0.1V	
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.4 2.2	-00	V A8	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	
V _{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0	[A	0.2 0.4 0.55	V 193	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 12 \text{mA}$ $I_{OL} = 24 \text{mA}$	
I	Input Leakage Current	2.7-3.6	5338	±5.0	μΑ	$0 \le V_1 \le 5.5V$	
loz	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V$ ($V_I = V_{LH} \text{ or } V_{CC}$)	
loff	Power Off Leakage Current	0		100	μΑ	$V_I \text{ or } V_O = 5.5V$	
Icc	Quiescent Supply Current	2.7-3.6	HID1	20	μΑ	$V_I = V_{CC}$ or GND	
			-	±20	μΑ	$3.6 \le (V_I, V_O) \le 5.5V_O$	
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μΑ	$V_{IH} = V_{CC} - 0.6V$	

See NS Package Number

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

	Parameter	Vcc		°C to +85°C 50 pF	Units
Symbol	Parameter	(V)	Min	Max (Note 2)	ILCX1
T _{PHL} , T _{PLH}	Propagation Delay Bus to Bus	2.7 3.0-3.6	1.5 1.5	6.6 6.0	ns
T _{PHL} , T _{PLH}	Propagation Delay Clock to Bus	2.7 3.0-3.6	1.5 1.5	noi ^{8.3}	ns
T _{PLH}	Propagation Delay SAB or SBA to A _n or B _n	2.7 3.0-3.6	1.5 1.5 1.5	8.3 T Hilliw 7.5	transmission to transmission transmission to transmission to transmission transmission transmi
T _{PZH} , T _{PZL}	Output Enable Time G to An or Bn (Assume Assume As	2.7 3.0-3.6	ne A oran bus will be opnate alors pin or	ne alsC8.3 elsper register 7.5 the app	ke 2n nto the
T _{PHZ} , T _{PLZ}	Output Disable Time G to A _n or B _n	2.7 3.0–3.6	1.5 itonut 1	7.5	provided to selections
T _{PZH} , T _{PZL} \$38	Output Enable Time DIR to An or Bn	2.7 3.0-3.6	1.5	7.5	ons with cap
T _{PHZ} , T _{PLZ}	Output Disable Time DIR to A _n or B _n	2.7 3.0–3.6	n nismism ^{1.5} nw noi 1.5	nego bs8.3 ngiri e	Son Achieved
ts	Setup Time VOBS < Isboth	3.0-3.6	2.5 2.5		ns
t _H	Hold Time	2.7 3.0-3.6	1.5 1.5	ode: See Section	eninsb
tw	Pulse Width 10510 11013	2.7 3.0-3.6	4.0 4.0	lodi	nya olog ns
T _{OSHL} , T _{OSLH}	Output to Output Skew (Note 1)	3.0	11111	1.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

	70c - 77 - 50 - Voc	Vcc	T _A = 25°C		6884	
Symbol	Parameter	(V)		Units	Conditions	
VOLP	Quiet Output Dynamic Peak VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	
VOLV	Quiet Output Dynamic Valley VOL	3.3	0.8	V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$	

Capacitance

Symbol	Parameter	Typical	Units	Conditions
CIN	Input Capacitance	7 33	os PFoa	$V_{CC} = Open$ $V_{I} = OV \text{ or } V_{CC}$
C _{1/O}	Input/Output Capacitance	8 XCITI	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
C _{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$



PRELIMINARY CONTROL See Section 2 for Test Metho

74LCX16652

Low-Voltage Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX16652 contains sixteen non-inverting bidirectional bus transceivers with TRI-STATE® outputs providing multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to the HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

The LCX16652 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment

The LCX16652 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

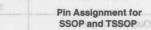
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7 to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SSOP and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16652
- Latch-up performance exceeds 300 mA
- ESD performance:

Human Body Model > 2000V Machine Model > 250V

Ordering Code: See Section 11

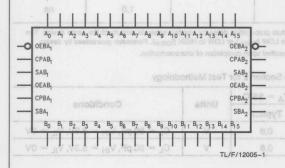
Logic Symbol

Connection Diagram



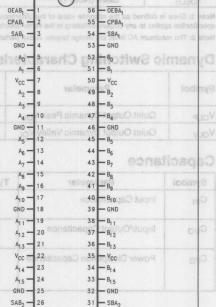
CPAB₂ - 27

OEAB₂



	SSOP EIAJ VO	74LCX16652MTD 74LCX16652MTDX	
Order Number	74LCX16652MEA 74LCX16652MEAX		
See NS Package Number	MS56A	MTD56	

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.



30 - CPBA₂

29 - OEBA

TL/F/12005-2

Logic Diagram

Functional Description

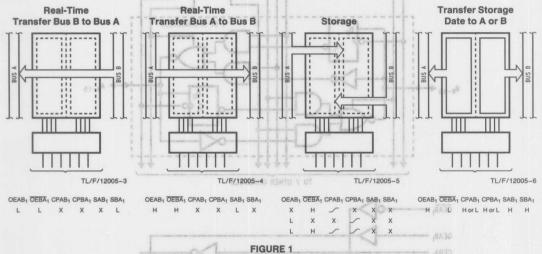
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both.

The select (SAB_n, SBA_n) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the 74LCX16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the ap-

propriate Clock Inputs (CPAB_n, CPBA_n) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB_n and OEBA_n. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.



Function Table (Note)

Inputs			-	Inputs/Outputs		SAZOperating Mode			
OEAB ₁	OEBA ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA ₁	A ₀ thru A ₇	B ₀ thru B ₇	ancoperating mode	
L	Н	H or L	HorL	X	X	Input	Input	Isolation	
L	Н	1	1	X Do	X	ST3NNV	Input	Store A and B Data	
Χ	Н	1	H or L	X 0-	×	Input	Not Specified	State A, Hold B	
Н	Н	1	~	X	X	Input	Output	Store A in Both Registers	
L	X	H or L	5	X	X	Not Specified	Input	Hold A, Store B	
L	L	1	5	X	×	Output	Input	Store B in Both Registers	
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	
L	L	X	H or L	X	H	- Gupur	i i	Store B Data to A Bus	
Н	Н	X	X	L	X		Outrot	Real-Time A Data to B Bus	
Н	Н	HorL	X	Н	X	Input	Output	Stored A Data to B Bus	
H2-900	JUF/12	H or L	H or L	H n bluoria ism	CHANNELS H operations	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus	

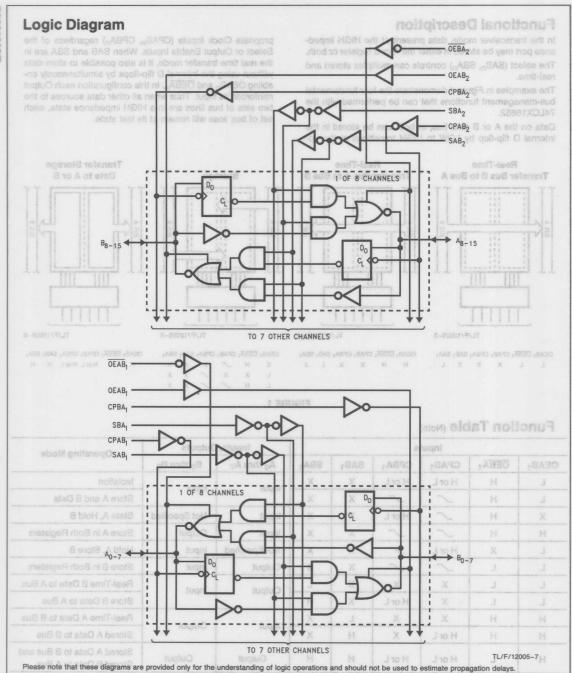
H = HIGH Voltage Level

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8–15) and #2 control pins.

L = LOW Voltage Level

X = Immaterial

⁼ LOW to HIGH Clock Transition



levs.I egalloV HQIH = H levs.I egalloV WQI = J

X = limmalerial

Note: The data output functions may be enabled or doubled by various signals at OEAS or OEBA inputs. Data trout functions are always enabled, i.e., data at the

emiT bloH

Propaga Bus to B	2.0V to 3.6V 1.5V to 3.6V 0V to 5.5V
	0\/ to E E\/
	0 V 10 5.5 V
	трен
Propaga Glock to	0V to V _{CC} 0V to 5.5V
-	14,749
Propaga SAB or 8	± 24 mA ± 12 mA
T _A) au 0 -	-40°C to +85°C
	10 ns/V
A STATE OF THE PARTY OF T	
	Zhdi,
	ls st
2	OEAR to Output Doutput

DC Electrical Characteristics **

fine the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

VI = OV OF VOC

Cumbal	Symbol Parameter V _{CC}		$T_A = -40^{\circ}\text{C to} + 85^{\circ}\text{C}$			Conditions
Symbol	Parameter	(V)	Min 0.8	Max	Units	of the Conditions of Hugos
device. "HIV	High Level Input Voltage	2.7-3.6	ong lauto2.0tt massits	december of the difference b	v stulgeds si	V _{OUT} ≤ 0.1V or
VIL design	Low Level Input Voltage	2.7-3.6	either HIGH to LOW (0.8	touts witten	V _{OUT} ≤ 0.1V or ≥ V _{CC} − 0.1V
V _{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	V _{CC} - 0.2 2.2 2.3 2.4 2.2	haracterist	o phine	$I_{OH} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OH} = -18 mA$ $I_{OH} = -24 mA$
V _{OL}	Low Level Output Voltage	2.7-3.6	(V) Typics	0.2	Paramet	$I_{OL} = 100 \mu A$
V0 = J1V	$C_{L} = 50 \text{ pF, V}_{IH} = 3.3 \text{V}_{IH}$	2.7	8.8 0.8	0.4 0.55	out Dynam	I _{OL} = 12 mA I _{OL} = 24 mA
1 VO = 11V	Input Leakage Current	2.7-3.6	3,3 0.6	± 5.0	μА	0 ≤ V _I ≤ 5.5V
loz	TRI-STATE I/O Leakage	2.7-3.6		±5.0	μΑ	$0 \le V_O \le 5.5V$ $V_I = V_{IH} \text{ or } V_{IL}$
I _{OFF}	Power Off Leakage Current	0		100	μΑ	$V_1 \text{ or } V_0 = 5.5V$
Icc	Quiescent Supply Current	2.7-3.6	Typical	20	μА	$V_I = V_{CC}$ or GND
	V _{OC} = Open	1 19	7	±20	μА	$3.6 \le (V_I, V_O) \le 5.5$
ΔI _{CC}	Increase in I _{CC} per Input	2.7-3.6		500	μА	$V_{IH} = V_{CC} - 0.6V$
	V _I = 0V or V _{CC}	Aq	8			0,10
	Vcc = 3.3V	Rq	32	n Capacitance	w Dissipatio	Cpp Powe

AC Electrical Characteristics: See Section 2 for Test Methodology 115 4 municipal Action 2 for Test Methodology 1 for Test Methodology 1

Symbol	Parameter	Condition Supplemental Control	$T_{A} = -40^{\circ}C_{L} =$	Units	
2.0V to 3.6V	tion Only	C(V) rating Data Reter	-0,5/ niM +7,0V	Max (Note 2)	Supply Volta
VtpHL01 V0 tpLH	Propagation Delay Bus to Bus	3.0-3.6	V0.V + 1.5/2.0 - 1.5		OC Input Vo an Volt
t _{PHL} V	Propagation Delay Clock to Bus	2.7 3.0–3.6	Ve.0 + 1.5 ve.0 - 1.5	8.3 belaisen cive (Note 6.8	Outputs 1 Carputs A
A ^t PHLS ±	Propagation Delay SAB or SBA to A _n or B _n	2.7 3.0–3.6	1.5 Am 0a-1.5	(HOI)8,30mmO eboid	snutput OC
t _{PZH}	Output Enable Time OEBA to An or Bn		Am 03 1.5 Am 03 1.5	1.0	No > Vod
t _{PHZ}	Output Disable Time OEBA to A _n or B _n	2.7 3.0–3.6	Am 00 1.5	8.3 (an 7.5) nig v	10 00 V OC Iqque ns I
t _{PZH}	Output Enable Time OEAB to A _n or B _n	2.7 3.0-3.6	1.5	8.3 7.5	en Vote 1: The
t _{PHZ}	Output Disable Time OEAB to A _n or B _n	2.7 3.0-3.6		the sake,80° the devi- soice shoul 2.7° the operat	
ts	Setup Time	2.7 3.0-3.6	2.5	allos delitied in the Lieu it guaranteed at the abso nmended Operation Con	able are no che 'Reco
t _H	Hold Time	2.7 3.0-3.6	nust be 0.2.1 must be 0.2.1	ditions for actual device of Absolute Maximum Rating	No ene cor
t _W	Pulse Width	2.7 3.0–3.6	4.0 solisin 4.0	ctrical Characte	ola na O
tosheetibaro	Output to Output Skew (Note 1)	3.0	Vcc (V)	Parameter	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

2.7-3.6 V_{CG} - 0.2

High Level Output Voltage

TRI-STATE I/O Leakage

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	ot = Jol Parameter 8.0	V _{CC} (V)	Typical	Units	egatioV tuqtuc Conditions
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	0.8	0.E V	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$
Volv va	Quiet Output Dynamic Valley VOL	3.3	0.8	No. 7-8	$C_L = 50 \text{ pF}, V_{IH} = 3.3 \text{V}, V_{IL} = 0 \text{V}$

Capacitance

10H = -100 MA

Symbol	Parameter	Typical	Units	Conditions
/d.d 2 (0V ,(V)	Input Capacitance	7	0.8-7.1 pF	V _{CC} = Open V _I = 0V or V _{CC}
C _{I/O}	Input/Output Capacitance	8	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$
C _{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3V$ $V_{I} = 0V \text{ or } V_{CC}$ $F = 10 \text{ MHz}$



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	Outputs

Section 6 LVX Translator Family

6



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Section 6 LVX Translator Family





LVX Translator Family Low Voltage Dual Supply CMOS Translating Transceivers

eatures	neuerai nescribitori		
Features Truitiv addiscrepa street	Advantages Advantages		
Advanced 0.8 µm CMOS process bas bog A is woll also VE	Propagation delays as fast as 7 ns maximum ValVE bexim a ril		
Bi-directional interface between 3V and 5V system 100 should be a second should be a seco	Works as bus transceiver in 3V/5V mixed systems and also works like a 74 series 245 in the single supply system		
±24 mA drive current ascardage 9CSD and OIOS in ediable VA	Balanced drive, guaranteed incident wave switching into 50 $\Omega_{\rm c}$ transmission line of S HBHs in ment gapsag vs area 3 bas		
Extended V_{CC} range from 2.7V to 3.6V, compatible with January JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation		
Low standby current (50 μA) maximum	Saves power, extends battery life may are fugured stonds on as		
Patented Quiet Series noise reduction circuitry	Guaranteed simultaneous switching noise level and dynamic threshold performance		
Flexible V _{CCB} operating range in Configurable Transceiver (LVXC)	Fits both 3V and 5V PCMCIA cards 19000 grilli9010		
B ports and V _{CCB} allowed to float with Configurable Transceiver (LVXC)	Allows plug and remove PCMCIA cards freely		
SOIC and QSOP packaging	Saves board space and weight		

Description	Pin Names
Output Enable Input	30
Transmit/Receive Input	A)T
Side A Inputs or TRI-STATE Outputs	TA-0A
Side B Inputs or TRI-STATE Outputs	60-87

	SOIC JEDEC	
74LVX3245QSC 74LVX3245QSGX	74LVX3245WM 74LVX3245WMX	Order Number
MQA24		See NS Package Number



74LVX3245 8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

The LVX3245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 3V bus and a 5V bus in a mixed 3V/5V supply environment. The Transmit/Receive (T/R) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 3V bus; the B port interfaces with the 5V bus.

The LVX3245 is suitable for mixed voltage applications such as notebook computers using 3.3V CPU and 5V peripheral components.

Features

- Bidirectional interface between 3V and 5V buses
- Inputs compatible with TTL level
- 3V data flow at A port and 5V data flow at B port
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages MSNUO evil Am
- Implements proprietary EMI reduction circuitry
- Functionally compatible with the 74 series 245

Ordering Code: See Section 11 V3 bas V6 drod et 3

Logic Symbol shap AIOMOS everies bus pulo ewella

OE A₀ A₁ A₂ A₃ A₄ A₅ A₆ A₇ T/R B₀ B₁ B₂ B₃ B₄ B₅ B₆ B₇ TL/F/11620-1

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11620-2

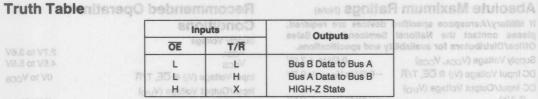
EC Std. No. 8-18

(LVX(C)

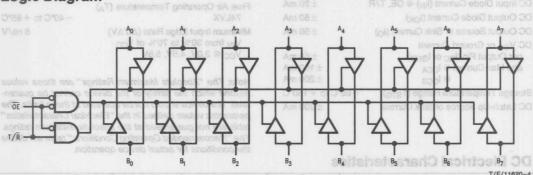
Pin Names	Description					
ŌĒ	Output Enable Input					
T/R	Transmit/Receive Input					
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs					
B ₀ -B ₇	Side B Inputs or TRI-STATE Outputs					

	SOIC JEDEC	QSOP
Order Number	74LVX3245WM 74LVX3245WMX	74LVX3245QSC 74LVX3245QSCX
See NS Package Number	M24B	MQA24

DC Input Didde Current (Ing) @ OE, T/R



Logic Diagram



		20	7	-2	-3		41161161	55 IBITO PEGITION	F/11620-4
		74LVX3245		ZALVX				"	F/1102U-4
Conditions	Unite	T _A = -40°C to +85°C	25°C	+ = AT	Voca (V)			Parameter I	
			Guara	qy7					
V _{OUT} ≤ 0.1V or ≥ V _{OC} = 0.1V		2.0 2.0	2.0		5.0 5.0		Nimum A(n), TXR, ph Level OE		
		2.0	2.0		4.5 5.5	3.8		Input Voltage	8HI
			8.0		5.0 5.0			Maximum Low Level Input Voltage	A.B
		8.0 8.0			4.5 5.5				
$I_{OUT} = -100 \mu A$ $I_{OH} = -24 m A$ $I_{OH} = -12 m A$ $I_{OH} = -12 m A$ $I_{OH} = -24 m A$			2.9 2.3 2.3 2.1	2.99 2.65 2.5 2.3	4.5 4.5 4.5 4.5	3.0 3.0 2.7 2.7	Minimum High Level Output Voltage		AHO
$l_{OUT} = -100 \mu A$ $l_{OH} = -24 \text{ mA}$	V	4.4	4,4 3,86	4.5 4.25	4.5 4.5				
$l_{OUT} = 100 \mu A$ $l_{OL} = 24 m A$ $l_{OL} = 12 m A$ $l_{OL} = 24 m A$		0.1 0.44 0.5	0.1 0.36 0.36 0.42	0.002 0.21 0.11 0.22	4.5 4.5 4.5 4.5		Maximum Low Level Output Voltage		
lour = 100 µA lou = 24 mA		0.1	0.1	0.002	4.6				
		0.f±			a.a	3.6		Maximum Input Leakage Current e OE, T/R	V
						3.6		Maximum TRI-STATE Output Leakage © A(n)	AZC

please contact the National Office/Distributors for availabili	
Supply Voltage (V _{CCA} , V _{CCB})	-0.5V to $+7.0$ V
DC Input Voltage (VI) @ OE, T/R	$-0.5V$ to $V_{CCB} + 0.5V$
DC Input/Output Voltage (VI/O)	HIGH-Z State
@ A(n)	-0.5V to V _{CCA} + 0.5V
@ B(n)	-0.5 V to $V_{CCB} + 0.5$ V
DC Input Diode Current (I _{IN}) @ OE,	T/R ± 20 mA
DC Output Diode Current (IOK)	±50 mA
DC Output Source or Sink Current	(I _O) ±50 mA
DC V _{CC} or Ground Current	
per Output Pin (I _{CC} or I _{GND})	±50 mA
and Max Current @ ICCA	± 100 mA
@ IccB	± 200 mA
Storage Temperature Range (TSTG	-65°C to +150°C
DC Latch-Up Source or Sink Curren	+300 mA

Supply Voltage	0.71/1-0.01/
VCCA	2.7V to 3.6V
VCCB	4.5V to 5.5V
Input Voltage (V _I) @ OE, T/R	0V to V _{CCB}
Input/Output Voltage (VI/O)	
@ A(n)	OV to V _{CCA}
@ B(n)	OV to V _{CCB}
Free Air Operating Temperature (T _A)	
74LVX	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$) V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	8 ns/V

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

					74LVX	(3245	74LVX3245		
Symbol	Paramete	r	V _{CCA} (V)	V _{CCB} (V)	T _A = -	+ 25°C	T _A = -40°C to +85°C	Units	Conditions
					Тур	Guara	anteed Limits		
V _{IHA}	Minimum High Level	$A(n), T/\overline{R},$ \overline{OE}	3.6 2.7	5.0 5.0		2.0 2.0	2.0		$V_{OUT} \le 0.1 V$ or $\ge V_{CC} - 0.1 V$
V _{IHB}	Input Voltage	B(n)	3.3 3.3	4.5 5.5		2.0 2.0	2.0 2.0	v	
V _{ILA}	Maximum Low Level Input Voltage	A(n), T/R,	3.6 2.7	5.0 5.0		0.8 0.8	0.8 0.8		$V_{OUT} \le 0.1V$ or $\ge V_{CC} - 0.1V$
V _{ILB}		B(n)	3.3 3.3	4.5 5.5		0.8	0.8 0.8	V	
V _{OHA}	Minimum High Level Output Voltage		3.0 3.0 2.7 2.7	4.5 4.5 4.5 4.5	2.99 2.65 2.5 2.3	2.9 2.35 2.3 2.1	2.9 2.25 2.2 2.0	٧	$I_{OUT} = -100 \mu A$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
V _{OHB}			3.0 3.0	4.5 4.5	4.5 4.25	4.4 3.86	4.4 3.76	٧	$I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -24 \text{mA}$
VOLA	Maximum Low Level Output Voltage		3.0 3.0 2.7 2.7	4.5 4.5 4.5 4.5	0.002 0.21 0.11 0.22	0.1 0.36 0.36 0.42	0.1 0.44 0.44 0.5	٧	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
V _{OLB}			3.0 3.0	4.5 4.5	0.002 0.18	0.1 0.36	0.1 0.44	٧	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$
I _{IN}	Maximum Input Leakage Current @ OE, T/R		3.6	5.5		±0.1	±1.0	μΑ	$V_I = V_{CCB}$, GND
loza	Maximum TRI-STATE Output Leakage @ A(n)		3.6	5.5		±0.5	±5.0	μΑ	$V_{I} = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_{O} = V_{CCA}, GNE$

	a	Ξ	٦	
r	ø	а		
	4	×	Я	

Symbol	Param	eter	V _{CCA} (V)	V _{CCB}	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Conditions
Dillo	=2.77	Yeer			Тур	Guar	anteed Limits		
lozB	Maximum TRI- Output Leakag @ B(n)	(913/6	3.6	5.5	nilli 0.1	±0.5	## ±5.0	μΑ	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}, GND$
Δlcc	Maximum	B(n)	3.6	5.5	1.0	1.35	1.5	mA	$V_I = V_{CCB} - 2.1V$
an.	I _{CCT} /Input @	A(n), T/R,	3.60.8	5.5	1.0	0.35	0.5	mA	$V_I = V_{CCA} - 0.6V$
ICCA	Quiescent V _{CC} Supply Current	73 7	3.6	5.5	0.1	5	8 8.A 0 50 8 8.a 0	μΑ	$ A(n) = V_{CCA} \text{ or GND} $ $ B(n) = V_{CCB} \text{ or GND,} $ $ \overline{OE} = \text{GND, } T/\overline{R} = \text{GND} $
ICCB	Quiescent V _{CC} Supply Current		3.63.8	5.5	1.0	8	0 6.8 7 0 6.8 7 0 6.2 7	μΑ	$ \begin{aligned} & A(n) = V_{CCA} \text{ or GND} \\ & B(n) = V_{CCB} \text{ or GND,} \\ & \overline{OE} = GND, T/\overline{R} = V_{CCA} \end{aligned} $
V _{OLPA} V _{OLPB}	Quiet Output N Dynamic V _{OL}	Maximum 0.1	3.3	5.0 5.0	1,0	0.8	0 6.3 8.0 0 3.7 6	V	(Notes 1, 2)
V _{OLVA}	Quiet Output N Dynamic V _{OL}	Minimum	3.3	5.0 5.0		-0.8 -1.2	1.0.1	V	(Notes 1, 2)
V _{IHDA} V _{IHDB}	Minimum High Dynamic Input		3.3	5.0 5.0		2.0		V _{va.o}	(Notes 1, 3)
V _{ILDA}	Maximum Low Dynamic Input	had suppredict our	3.3	5.0 5.0	olusi propu NO LOW	0.8	the difference being	ule Vilue, o	(Notes 1, 3)

†Maximum test duration 2.0 ms. one output loaded at a time.

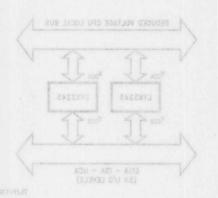
Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold

 (V_{ILD}) , f = 1 MHz.

V _{OC} = Open	Rg	4.5			
				Input/Output Capacitance	
				Power Dissipation	
			B → A		



8-Bit Dual Supply Translating Transceiver.
The LVX3245 is a dual supply device capable of bidirectionat signal translation. This level shifting ability provides an
efficient interface between low voltage CPU local bus with
memory and a standard bus defined by 6V I/O levels. The
device control inputs can be controlled by either the low
voltage CPU and core logic or a bus arbitrator with 6V I/O

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notabook computers using 3.3V CPU's and 6V peripheral devices.

	7	4LVX32	45	KSRA	V.1874L	VX3245		74L	VX3245	
Parameters etta	**\	A = +29 L = 50 CCA = CCB=5	pF 3.3V	7 25 G	**Vcc	0°C to + = 50 pF A = 3.3\ B = 5.0V	(V)	$T_A = -40^{\circ}\text{C to} + 85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$ $V_{CCA} = 2.7V$ * $V_{CCB} = 5.0V$		Units
V = V = V	Min	Тур	Max	14	Min	aa	Max	Min	Max	azo
Propagation Delay A to B	1.0	5.4 5.6	8.0 7.5	2.1	1.0	aa	8.5	1.0	9.0	ns
Propagation Delay B to A	1.0	5.1 5.7	7.5 7.5	6.0	1.0	5.5	8.0	7.1.0 A	8.5 augul 8.5	ns
Output Enable Time OE to B	1.0	4.8 6.3	8.0 8.5	2	1.0 1.0	aa	8.5 9.0	1.0 1.0	9.0 9.5	ns
Output Enable Time OE to A	1.0	6.3 6.8	8.5 9.0		1.0 1.0		9.0 9.5	1.0	9.5 10.0	ns
Output Disable Time OE to B	1.0 1.0	5.3 4.2	7.5 7.0	8	1.0 1.0	5.5	8.0 7.5	1.0 1.0	5.8 ly Current 0.8	ns
Output Disable Time OE to A	1.0 1.0	5.3 3.7	8.0 6.5	1.0	1.0 1.0	5.0 5.0	8.58.8 7.08.8	1.0 ixe	C.7. mio Vol	AS NO.
				1	Charles of the life		3.3			
- (Time OE to B Output Enable Time OE to A Output Disable Time OE to B Output Disable	Time OE to B 1.0 Output Enable 1.0 Time OE to A 1.0 Output Disable 1.0 Time OE to B 1.0 Output Disable 1.0	Time OE to B 1.0 6.3 Output Enable 1.0 6.3 Time OE to A 1.0 6.8 Output Disable 1.0 5.3 Time OE to B 1.0 4.2 Output Disable 1.0 5.3	Time OE to B 1.0 6.3 8.5 Output Enable 1.0 6.3 8.5 Time OE to A 1.0 6.8 9.0 Output Disable 1.0 5.3 7.5 Time OE to B 1.0 4.2 7.0 Output Disable 1.0 5.3 8.0	Time OE to B 1.0 6.3 8.5 Output Enable 1.0 6.3 8.5 Time OE to A 1.0 6.8 9.0 Output Disable 1.0 5.3 7.5 Time OE to B 1.0 4.2 7.0 Output Disable 1.0 5.3 8.0	Time OE to B 1.0 6.3 8.5 1.0 Output Enable 1.0 6.3 8.5 1.0 Time OE to A 1.0 6.8 9.0 1.0 Output Disable 1.0 5.3 7.5 1.0 Time OE to B 1.0 4.2 7.0 1.0 Output Disable 1.0 5.3 8.0 1.0	Time OE to B 1.0 6.3 8.5 1.0 Dutput Enable 1.0 6.3 8.5 1.0 Time OE to A 1.0 6.8 9.0 1.0 Output Disable 1.0 5.3 7.5 1.0 Time OE to B 1.0 4.2 7.0 1.0 Output Disable 1.0 5.3 8.0 1.0	Time OE to B 1.0 6.3 8.5 1.0 9.0 Dutput Enable 1.0 6.3 8.5 1.0 9.0 Time OE to A 1.0 6.8 9.0 1.0 9.5 Output Disable 1.0 5.3 7.5 1.0 8.0 Time OE to B 1.0 4.2 7.0 1.0 7.5 Output Disable 1.0 5.3 8.0 1.0 8.5 Time OE to A 1.0 3.7 6.5 1.0 7.0	Time OE to B 1.0 6.3 8.5 1.0 9.0 1.0 Output Enable 1.0 6.3 8.5 1.0 9.0 1.0 Time OE to A 1.0 6.8 9.0 1.0 9.5 1.0 Output Disable 1.0 5.3 7.5 1.0 8.0 1.0 Time OE to B 1.0 4.2 7.0 1.0 7.5 1.0 Output Disable 1.0 5.3 8.0 1.0 8.5 1.0 1.0	Time OE to B 1.0 6.3 8.5 1.0 9.0 1.0 9.5 Dutput Enable 1.0 6.3 8.5 1.0 9.0 1.0 9.5 Time OE to A 1.0 6.8 9.0 1.0 9.5 1.0 10.0 Output Disable 1.0 5.3 7.5 1.0 8.0 1.0 8.5 Time OE to B 1.0 4.2 7.0 1.0 7.5 1.0 8.0 Output Disable 1.0 5.3 8.0 1.0 8.5 1.0 9.0

^{*}Voltage Range 5.0V is 5.0V ±0.5V. **Voltage Range 3.3V is 3.3V ±0.3V.

Capacitance

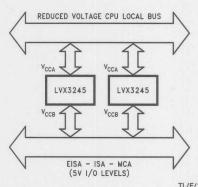
Symbol	GHIV) blorissidi Paramete	rdar-test switchin	Тур	Units	Conditions
CIN	Input Capacitance		4.5	pF	V _{CC} = Open
C _{I/O}	Input/Output Capacitance		15	pF	$V_{CCA} = 3.3V$ $V_{CCB} = 5.0V$
C _{PD}	Power Dissipation	$A \rightarrow B$	55	pF	V _{CCB} = 5.0V
	Capacitance	$B \rightarrow A$	40	Pi	V _{CCA} = 3.3V

C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX3245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



Hote 2: Max number of outputs defined as Note 3: Max number of Data inputs (n) swill

TL/F/11620-3

^{***}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.



74LVX4245

8-Bit Dual Supply Translating Transceiver with TRI-STATE® Outputs

General Description

The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive (T/\overline{R}) input determines the direction of data flow. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The A port interfaces with the 5V bus; the B port interfaces with the 3V bus.

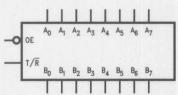
The LVX4245 is suitable for mixed voltage applications such as laptop computers using 3.3V CPU's and 5V LCD displays.

Features

- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A port and 3V data flow at B port
- Outputs source/sink 24 mA at 5V bus; 12 mA at 3V bus
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Functionally compatible with the 74 series 245

Ordering Code: See Section 11

Logic Symbol

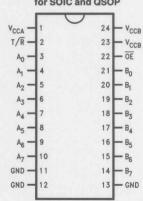


TL/F/11540-1

Pin Names	Description
ŌĒ	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs
B ₀ -B ₇	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11540-2

	SOIC JEDEC	QSOP
Order Number	74LVX4245WM	74LVX4245QSC
	74LVX4245WMX	74LVX4245QSCX
See NS Package Number	M24B	MQA24

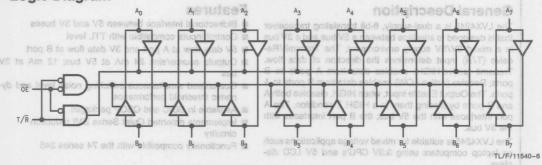
Truth Table

	Inp	uts	Outputs
	ŌĒ	T/R	Outputs 1012
	L	L	Bus B Data to Bus A
	L	Н	Bus A Data to Bus B
** VED-1	Hann	Y X	HIGH-Z State

74LVX4245

with TRI-STATE® Outputs

Logic Diagram



Connection Diagram





Ordering Code: See Seetlon 11

Logic Symbol

Description	Pin Names
Output Enable Input	
Transmit/Receive Input	
Side A Inputs or TRI-STATE Outputs	
Side B Inputs or TRI-STATE Outputs	80-87

9020	SOIC JEDEC	
74LVX4245QSC 74LVX4245QSCX	74LVX4245WM 74LVX4245WMX	Order Number
MQA24		See NS Package Number

Absolute Maximum Ratings (Note)	Recommended Operating
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage (V_{CCA} , V_{CCB}) $-0.5V$ to $+7.0V$ DC Input Voltage (V_{I}) @ \overline{OE} , T/\overline{R} $-0.5V$ to V_{CCA} + 0.5V	Conditions Supply Voltage VCCA VCCB Input Voltage (Vi) @ OE, T/R VCCA OV to VCCA
DC Input/Output Voltage (V _{I/O}) @ A(n) @ B(n) -0.5V to V _{CCA} + 0.5V -0.5V to V _{CCB} + 0.5V	Input/Output Voltage (V _{I/O}) TATE HTT WAR OV to VCCA @ A(n)
DC Input Diode Current (I _{IN}) ® OE, T/R ±20 mA DC Output Diode Current (I _{OK}) ±50 mA DC Output Source or Sink Current (I _O) ±50 mA DC V _{CC} or Ground Current	Free Air Operating Temperature (T_A) -40° C to $+85^{\circ}$ C Minimum Input Edge Rate ($\Delta t/\Delta V$) 8 ns/V V_{IN} from 30% to 70% of V_{CC}
per Output Pin (I _{CC} or I _{GND}) ±50 mA and Max Current @ I _{CCA} ±200 mA ±00 mA	Vcc @ 3.0V, 4.5V, 5.5V ADOV Inspection ADOV Inspection ADOV Inspection
Storage Temperature Range (T _{STG}) -65°C to +150°C DC Latch-Up Source or Sink Current ±300 mA Note: <i>The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaran-</i>	locs Oulescent Vocs 3.6 Supply Current 5.5 3.6
teed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics"	Vol.PA Quiet Output Maximum 5.0 3.3 Vol.PB Dynamic Vol. 5.0 3.3
table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	VOLVA Quiet Output Minimum 5.0 3.3 Volvg Dynamic Vol 5.0 3.3
DC Electrical Characteristics	VIHDA Minimum High Level 5.0 3.3

	(Notes 1, 3)			8.0	74LVX	4245	74LVX4245	I wo.J m	Val.DA Maximi
Symbol Parameter	V _{CC}		V _{CCB}	TA +25°C		$T_A = -40^{\circ}C$ to $+85^{\circ}C$	Units	Conditions	
		CUAL	In higher	some absorber	Тур	Guara	nteed Limits	okage.	Note It Worst case pa
VIHA	Minimum lorserti or level High Level	A(n), T/R,	5.5 4.5	3.3	V of V0 gnido	2.0	2.0 (n) s	Data Input	$V_{OUT} \le 0.1 \text{V or}$ $\ge V_{CC} - 0.1 \text{V}$
V _{IHB}	Input Voltage	B(n)	5.0 5.0	3.6 2.7		2.0 2.0	2.0 2.0	V	
V _{ILA}	Maximum Low Level Input Voltage	A(n), T/R, OE	5.5 4.5	3.3 3.3		0.8	0.8 0.8	V	V _{OUT} ≤ 0.1V or ≥ V _{CC} −0.1V
V _{ILB}		B(n)	5.0 5.0	2.7 3.6		0.8	0.8 0.8	V	
V _{OHA}	Minimum High Level Output Voltage		4.5 4.5	3.0 3.0	4.5 4.25	4.4 3.86	4.4 3.76	٧	$I_{OUT} = -100 \mu\text{A}$ $I_{OH} = -24 \text{mA}$
V _{OHB}			4.5 4.5 4.5	3.0 3.0 2.7	2.99 2.8 2.5	2.9 2.4 2.4	2.9 2.4 2.4	٧	$I_{OUT} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OL} = -8 mA$
V _{OLA}	Maximum Low Level Output Voltage		4.5 4.5	3.0 3.0	0.002 0.18	0.1 0.36	0.1 0.44	٧	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$
V _{OLB}			4.5 4.5 4.5	3.0 3.0 2.7	0.002 0.1 0.1	0.1 0.31 0.31	0.1 0.4 0.4	٧	$I_{OUT} = 100 \mu A$ $I_{OL} = 12 mA$ $I_{OL} = 8 mA$
I _{IN}	Maximum Input Leakage Current @ OE, T/R		5.5	3.6		±0.1	±1.0	μΑ	$V_I = V_{CCA}$, GND
loza	Maximum TRI-STATE Output Leakage @ A(n)		5.5	3.6		±0.5	±5.0	μΑ	$V_{I} = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_{O} = V_{CCA}, GND$

					rollib	74LV	X4245	7	4LVX4245	beltlase	my/Aerospade a		
Symbol Ve & Parameter	er	V _{CCA} (V)	V _{CCB}	T _A =	+25°C	A. 1. Cont. Co.	$\lambda = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Units	Conditions				
to Voca		Z ide	EXT	30 o 6	A anatlo	Тур	Gua	rante	ed Limits	AVT.	(Voltage (V)) © O		
lozb ADOV ot SOOV ot		um TRI-S : Leakage	1000	V) species 5.5	3.6	O\feqni A @ B @	±0.5		±5.0 0-	μΑ	$V_I = V_{IL}, V_{IH}$ $\overline{OE} = V_{CCA}$ $V_O = V_{CCB}, GN$	n)A Ø	
Δlcca		um I _{CCT} / , T/R, O		5.5	3.6	1.0	1.35	15	1.5	mA	$V_I = V_{CCA} - 2.$	1V	
7 1611 0	Input @	B(n)	of Vcc	5.5	3.6	VinV	0.35		0.5	mA	$V_I = V_{CCB} - 0.$	6V	
ICCA		ent V _{CC}	4	5.5	3.6	SOV	Am 08 Am 00	生	80	μA	$A(n) = V_{CCA}$ or $B(n) = V_{CCB}$ or $\overline{OE} = GND T/\overline{R}$	GND GND,	
ICCB		ent V _{CCI} Current	3	5.5	3.6		5	00 ; 16± 16000	50	μА	$A(n) = V_{CCA}$ or $B(n) = V_{CCB}$ or $\overline{OE} = GND T/\overline{R}$	r GND r GND,	
V _{OLPA} V _{OLPB}	Quiet (Output M	aximum	5.0 5.0	3.3 3.3		1.5		rated at thes lectrical Cha	V I	(Notes 1, 2)		
V _{OLVA} V _{OLVB}	Quiet (Output M	inimum	5.0 5.0	3.3 3.3		-1.2 -0.8	Non el	solute maxin ndificns" lab eracion.	V	(Notes 1, 2)	and are are one of the connection	
V _{IHDA} V _{IHDB}		ım High l		5.0 5.0	3.3 3.3		2.0		teristics	(Notes 1, 3)		E OG	
V _{ILDA} V _{ILDB}		um Low I		5.0	3.3	74LV0	0.8	V		٧	(Notes 1, 3)		
Note 1: Wo	orst case p ax number ax number o	ackage. of outputs	uts (n) switch	n). Data inp	uts are driv	ven 0V to V _{CC} ching 0V to V _C	CC level. Inpu	t-under-		CC level to	threshold (V _{IHD}), OV to	threshole	
(VILUM)	0002	V	0.5 0.5 0.5				9.9						
10 V1.0 0 V1.0 -	Vour ≤		8.0								Madmum Low L Input Voltage	AJ	
			8.0		8.0			5.0 5.0					
- 100 µJ - 24 mA		. V	1,4 .78		4.4 3.86	4.6		4.5					
- 100 pu - 12 mA 8 mA	HOI =	V					3.0 2.7	4.6 4.5 4.5					
Au 001 Am 65													
	lou = 1	٧				0.002 1.0 1.0	3.0	4,5 4,5 4,5					
	V = 1V	Ası	1.0		± 0.1							V	

Au

6

AC Electrical Characteristics: See Section 2 for Test Methodology

insceivar,	ured as an 8-bit 245 th ATE capabilities and the	74	LVX42	45	74LVX	1245	74LVX	4245	LVX4
Symbol Parameters Output Description Parameters Description Parameters Parameters		T _A = +25°C C _L = 50 pF *V _{CCA} = 5V **V _{CCB} = 3.3V			C _L = 5	0 pF so toubo	T _A = -40°C to +85°C C _L = 50 pF *V _{CCA} = 5V V _{CCB} = 2.7V		
	Company and the contract	Min	Тур	Max	Min s e	VE Max	inder niMot con		tor is
t _{PHL}	Propagation Delay A to B	1.0	5.1 5.3	8.5 8.5	1.0 1.0	9.0 9.0	spee 0.1 egrade the L0.1 245 or		o va
t _{PHL}	Propagation Delay B to A	1.0 1.0	5.4 5.5	8.5 8.5	1.0 ords 1		atri of f1.0 Va be abelia.0 of ho		ns ns
t _{PZL}	Output Enable Time OE to B	1.0	6.5 6.7	10.0	1.0 1.0	10.5 10.5	1.0	11.5 11.5	yadns
t _{PZL} t _{PZH}	Output Enable Time	1.0 1.0	5.2 5.8	9.0 9.0	1.0 1.0	9.5 9.5	1.0 1.0	10.0 10.0	ns
t _{PHZ}	Output Disable Time	1.0	6.0	9.5 6.5	1.0 1.0	10.0 7.0	1.0 1.0	10.0 7.5	ns
t _{PHZ}	Output Disable Time OE to A	1.0 1.0	3.9	7.0 6.5	1.0 1.0	7.5 7.0	1.0 1.0	7.5 7.5	ns
toshl toslh	Output to Output Skew*** Data to Output		1.0	1.5	IANNEL/	1.5 10090IM		1.5	ns

^{*}Voltage Range 5.0V is 5.0V \pm 0.5V.

Capacitance

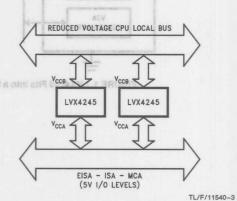
Symbol	Paramete		Тур	Units	Conditions
CIN	Input Capacitance		4.5	pF	V _{CC} = Open
C _{I/O}	Input/Output Capacitance	- d	15	LVX4245	$V_{CCA} = 5.0V$ $V_{CCB} = 3.3V$
C _{PD}	Power Dissipation	$B \rightarrow A$	55	pF	$V_{CCA} = 5.0V$
Capacitance		$A \rightarrow B$	40	pF	V _{CCB} = 3.3V

C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

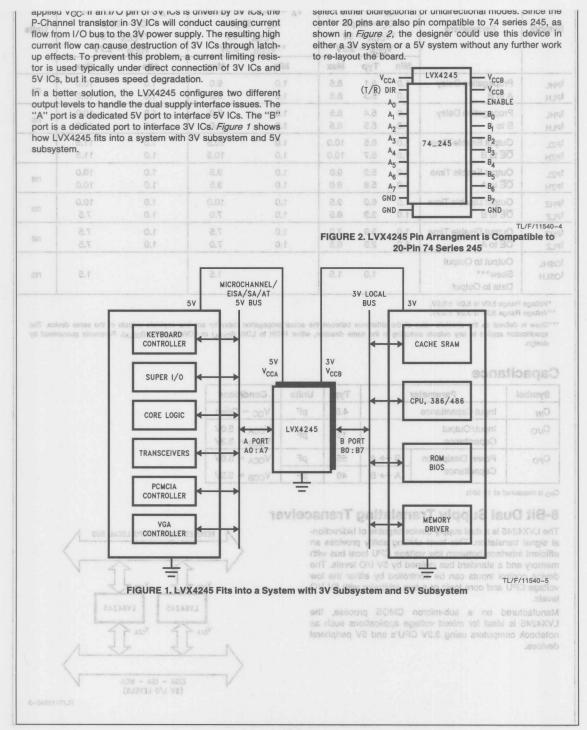
Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



6-13

^{**}Voltage Range 3.3V is 3.3V ±0.3V.

***Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by





74LVXC3245

8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs for 3V System

General Description

The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The $V_{\rm CCA}$ pin accepts a 3V supply level. The A port is a dedicated 3V port. The $V_{\rm CCB}$ pin accepts a 3V-to-5V supply level. The B port is configured to track the $V_{\rm CCB}$ supply level respectively. A 5V level on the $V_{\rm CC}$ pin will configure the I/O pins at a 5V level and a 3V $V_{\rm CC}$ will configure the I/O pins at a 3V level. The A port should interface with a 3V host system and the B port to the card slots. This device will allow the $V_{\rm CCB}$ voltage source pin and I/O pins on the B port to float when $\overline{\rm OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Bidirectional interface between 3V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when OE is HIGH
- Functionally compatible with the 74 series 245

Ordering Code: See Section 11

Logic Symbol



TL/F/12008-1

Pin Names	Description
ŌĒ	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs
B ₀ -B ₇	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for SOIC and QSOP



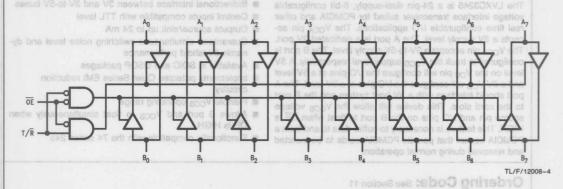
TL/F/12008-2

	SOIC JEDEC	QSOP 74LVXC3245QSC 74LVXC3245QSCX		
Order Number	74LVXC3245WM 74LVXC3245WMX			
See NS Package Number	M24B	MQA24		

Truth Table

	uts	Outputs	Semiconduction		
ŌĒ	T/R	Outputs	CATOO INTERNATIONS		
L	L	Bus B Data to Bus A	74LVXC3245		
L	H	Bus A Data to Bus B			
Н	X	HIGH-Z State	8-Bit Dual Su		
	DE L L	L L	OE T/R L L Bus B Data to Bus A L Bus A Data to Bus B		





Connection Diagram





General Description

Description			
Transmit/Receive Input			
Side A Inputs or TRI-STATE Outputs	7A-0A		
Side B Inputs or TRI-STATE Outputs			

SOIC JEDEC				
74LVXC3245WM 74LVXC3246WMX				
	See NS Package Number			

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Office/Distributors for availability	and specifications.
Supply Voltage (V _{CCA} , V _{CCB})	-0.5V to $+7.0$ V
DC Input Voltage (V _I) @ OE, T/R	-0.5V to V _{CCA} +0.5V
DC Input/Output Voltage (V _{I/O}) @ A _n @ B _n	-0.5V to V _{CCA} +0.5V -0.5V to V _{CCB} +0.5V
DC Input Diode Curr. (IIK) @ OE, T/R	± 20 mA
DC Output Diode Current(I _{OK})	±50 mA
DC Output Source or Sink Current (Ic	±50 mA
DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) and Max Current	± 50 mA ± 200 mA
Storage Temperature Range (TSTG)	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating

Supply Voltage V _{CCA}	2.7V to 3.6V (V _{CCA} ≤ V _{CCB})
(v) V _{CCB}	3.0V to 5.5V
Input Voltage (VI) @ OE, T/R	0V to V _{CCA}
Input Output Voltage (V _{I/O}) @ A _n @ B _n	0V to V _{CCA} 0V to V _{CCB}
Free Air Operating Temperature (T _A)	-40°C to +85°C
Willimum input Euge hate (AV/At)	Output Lea

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

	An = Voca er G		50	V _{CCB}	74LVX	C3245	74LVXC3245		CCA2 Quiescent
Symbol TVT, GM Parame		V _{CCA}	T _A =		25°C	T _A = -40°C to +85°C	Units	Conditions	
A _B = V _{GGA} or GVD,		An	08	8	Тур	Gua	ranteed Limits	Vccs	XCs Culescent
V _{IHA} V =	Minimum High	A _n ,	2.7	3.0		2.0	2.0	3130	and fulling
	Level Input Voltage	OE VT/R	3.0 3.6	3.6 5.5		2.0	2.0		V _{OUT} ≤ 0.1V or ≥ V _{CC} − 0.1V
V _{IHB}	(Notes 1, 2)	B _n	2.7 3.0 3.6	3.0 3.6 5.5		2.0 2.0 3.85	2.0 2.0 3.85		
V _{ILA}	Maximum Low Level Input Voltage	A _n , OE T/R	2.7 3.0 3.6	3.0 3.6 5.5		0.8 0.8 0.8	0.8 0.8 0.8	ynamic	V _{OUT} ≤ 0.1V
V _{ILB}	(Notes 1, 3)	Bn	2.7 3.0 3.6	3.0 3.6 5.5		0.8 0.8 1.65	0.8 0.8 1.65		or ≥Vcc - 0.1V Hamming AGH
V _{OHA}	Minimum High L Output Voltage	evel	3.0	3.0 3.0	2.99 2.85	2.9 2.56	2.9 2.46	96	$I_{OUT} = -100 \mu$ $I_{OH} = -12 \text{mA}$
	(Notes 1, 3)	V	3.0 2.7	3.0	2.65 2.5	2.35	2.25 2.2	V wo.	$I_{OH} = -24 \text{ mA}$ $I_{OH} = -12 \text{ mA}$
V _{OHB}	(Notes 1, 3)	V	3.0	3.0	2.3	2.1	2.0	98	$I_{OH} = -24 \text{ mA}$ $I_{OUT} = -100 \mu A$
blodaswii ot	VQ (musV) hindework or	nor Voc love	3.0 3.0 3.0	3.0 3.0 4.5	2.85 2.65 4.25	2.56 2.35 3.86	2.46 2.25 3.76	V _{agas} ,V	$I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
VOLA	Maximum Low Level Output Voltage		3.0 3.0 2.7 2.7	3.0 3.0 3.0 4.5	0.002 0.21 0.11 0.22	0.1 0.36 0.36 0.42	0.1 0.44 0.44 0.5	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
V _{OLB}		3.0 3.0 3.0	3.0 3.0 4.5	0.002 0.21 0.18	0.1 0.36 0.36	0.1 0.44 0.44	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	

DC Electrical Characteristics (Continued)

			HOH	ipno.	74LVX	(C3245	74LVXC3245	lenol	y/Aerospace spa contact the Nat		
Symbol	Parameter V0.6	VCCA VCCB	V _{CCA} (V)	V _{CCB} (V)	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Supply Voltage (Voca, Voca)		
ADDV 0	t V0	A\T,3€ e	(V) age	noV juq	Typ Guaran		inteed Limits	FIT	DC Input Voltage (V₂) @ ÖE,		
NOCA O VOCB	Maximum Input Leakage Current @ OE, T/R	age (V _I /O)	3.6 3.6	3.6 5.5	tl a	±0.1 ±0.1	∞V ±1.00- ∞V ±1.00-	μA μΑ	$V_{I} = V_{CCA}$, GND	DC Input © An © Bn	
loza _{an 8}	Maximum TRI-STATE Output Leakage @ An	ige Rate (Δ\ to 70% of V 5V, 5,5V	3.6 3.6	3.6 5.5	M	±0.5 ±0.5	±5.0 ±5.0	μА	$V_{I} = V_{IL}, V_{IH},$ $\overline{OE} = V_{CCA}$ $V_{O} = V_{CCA}, GNE$		
OZB SEVISV -NSYBUT SAT ST	Maximum TRI-STATE Output Leakage @ Bn	lute Maximu e safety of a	3.6	3.6 5.5	N d	±0.5 ±0.5	±5.0 ±5.0	µА (Тата	$V_{I} = V_{IL}, V_{IH},$ $\overline{OE} = V_{CCA}$ $V_{O} = V_{CCB}, GNE$	and Ma Storage	
Δlcc	Maximum	Bn	3.6	5.5	1.0	1.35	1.5	Curren	$V_I = V_{CCB} - 2.1V$		
atings.	I _{CC} /Input	All Inputs	3.6	3.6	10	0.35	0.5	mA	$V_I = V_{CC} - 0.6V$		
ICCA1	Quiescent V _{CCA} Supply Current as B Port Floats	actual devi	3.6	Open	13	5	50	μА	$A_n = V_{CCA} \text{ or GN}$ $B_n = \text{Open, } \overline{\text{OE}} = \text{T/}\overline{\text{R}} = V_{CCA}, V_{CCA}$	= V _{CCA} ,	
loca2	Quiescent V _{CCA} Supply Current	- 40°C	3.6 3.6	3.6 5.5	74LV) TA =	5	50 50	μА	$\begin{aligned} &A_n = V_{CCA} \text{ or GN} \\ &B_n = V_{CCB} \text{ or GN} \\ &\overline{OE} = \text{GND, T/R} \end{aligned}$	ND,	
Іссв	Quiescent V _{CCB} Supply Current	d Umits 2.0	3.6 3.6	3.6	gyT	5 8.8	50 80	μA	$\begin{aligned} &A_n = V_{CCA} \text{ or GN} \\ &B_n = V_{CCB} \text{ or GN} \\ &\overline{OE} = \text{GND, T/R} \end{aligned}$	ND,	
VOLPA	Quiet Output Maximum Dynamic	2.0	3.3 3.3	3.3 5.0		0.8	8.8	NTV	(Notes 1, 2)		
VOLPB	Vol	2.0	3.3 3.3	3.3 5.0		0.8	3.0	V	(Notes 1, 2)	8HIV	
V _{OLVA}	Quiet Output Minimum Dynamic	8.0	3.3 3.3	3.3 5.0		-0.8 -0.8	2.7	AV	(Notes 1, 2)	AJIV	
V _{OLVB}	VOLV	8.0	3.3 3.3	3.3 5.0		-0.8 -1.2	3.6	VTV	(Notes 1, 2)		
VIHDA	Minimum High Level Dynamic	0.8	3.3 3.3	3.3 5.0		2.0	0.6	٧	(Notes 1, 3)	STILE.	
VIHDB 1	Input Voltage	2.9	3.3 3.3	3.3	2.99	2.0 3.5	0.0	V	(Notes 1, 3)	AHOV	
VILDA	Maximum Low Level Dynamic	2.25	3.3 3.3	3.3 5.0	2.65 2.5	0.8	2.7	V	(Notes 1, 3)		
V _{ILDB}	Input Voltage	2.0	3.3	3.3	6.5	0.8	7.5		(Notes 1, 3)	7	

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to VCC level. Input-under-test switching: VCC level to threshold (V_{IHD}), 0V to threshold $(V_{ILD}), f = 1 MHz.$

Amst = Jol $l_{OL} = 24 \, mA$

0.36

AC Electrical Characteristics: See Section 2 for Test Methodology and AC AC ACT See Section 2 for Test Methodology

		74LVXC3245 T _A = +25°C C _L = 50 pF V _{CCA} = 2.7V-3.6V V _{CCB} = 4.5V-5.5V			74L	VXC3245	74LV	XC3245	74LV)	C3245	EG!
Symbol	Parameter				C _L	0°C to +85°C = 50 pF = 2.7V-3.6V = 4.5V-5.5V	C _L =	+ 25°C = 50 pF 2.7V-3.6V 3.0V-3.6V			Units
		Min	Typ (Note 1)	Max	Min	Max (and	Min (Not		Min	Max	
t _{PHL}	Propagation Delay A to B	1.0 1.0	4.8	8.0 6.5	1.0	8.5 7.0	1.0 5. 1.0 5.		1.0	9.0 8.5	ns
t _{PHL}	Propagation Delay B to A	1.0 1.0	3.8 4.3	6.5 7.5	1.0 1.0	7.0 8.0	1.0 4. 1.0 5.		1.0	7.5 8.0	ns
t _{PZL}	Output Enable Time OE to B	1.0	4.7 4.8	8.0 8.5	1.0	8.5 9.0	1.0 6. 1.0 6.	4 3	1.0	9.5 10.0	ns
t _{PZL}	Output Enable Time OE to A	1.0	5.9 5.4	9.5 9.0	1.0	10.0 9.5	1.0 6. 1.0 5.		1.0	10.5 9.5	ns
t _{PHZ}	Output Disable Time OE to B	1.0	4.0	8.0 7.5	1.0	8.5 8.0	1.0 6. 1.0 4.		1.0	10.0 8.5	ns
t _{PHZ}	Output Disable Time OE to A	1.0 1.0	4.6 3.1	9.5 6.5	1.0 1.0	10.0 7.0	1.0 5. 1.0 3.		1.0 1.0	10.0 7.0	ns
toshl toslh	Output to Output Skew* Data to Output	SLOT	1.0	1.5		1.5	102 A.	0 1.5	7	1.5	ns

Note 1: Typical values at V_{CCA} = 3.3V, V_{CCB} = 5.0V @ 25°C.

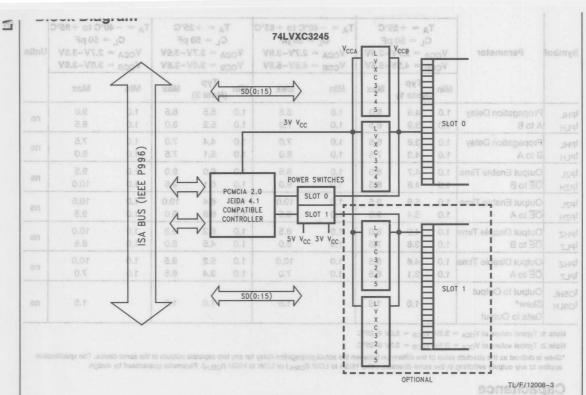
Note 2: Typical values at V_{CCA} = 3.3V, V_{CCB} = 3.3V @ 25°C.

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

Capacitance

Symbol	Paramete	THE VOCA PERCE	Тур	Units	Conditions	ne LVXC3245 is a 24 g CMCIA configurable
CIN BOOV	Input Capacitance	itance and bebeen segments 4.5 and 6		seepForm	V _{CC} = Open	notebook designs, th
CI/O	Input/Output Capacitanc	the voltage and dard (IEEE 2996	108 8	note equation of the period of	$V_{CCA} = 3.3V$ $V_{CCB} = 5.0V$	mW of quiescent po VXC3245 meets all FO V and 3.3V operation
C _{PD}	Power Dissipation	$A \rightarrow B$	50	P P P	$V_{CCB} = 5.0V$	ne card voltage supply,
	Capacitance	$B \rightarrow A$	40	pF	$V_{CCA} = 3.3V$	ence rail to rail output

C_{PD} is measured at 10 MHz.



The LVXC3245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC3245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V $_{\rm CCB}$ of the LVXC3245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC3245 must always be tied to a 3V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).



74LVXC4245

8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs

General Description

The LVXC4245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 5V supply level. The "A" port is a dedicated 5V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The "B" port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. This device will allow the V_{CCB} voltage source pin and I/O pins on the "B" port to float when $\overline{\rm OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Bidirectional interface between 5V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when OE is HIGH
- Functionally compatible with the 74 series 245

Ordering Code: See Section 11

Logic Symbol

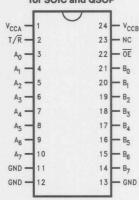


TL/F/12009-1

Pin Names	Description							
ŌĒ	Output Enable Input							
T/R	Transmit/Receive Input							
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs							
B ₀ -B ₇	Side B Inputs or TRI-STATE Outputs							

Connection Diagram

Pin Assignment for SOIC and QSOP



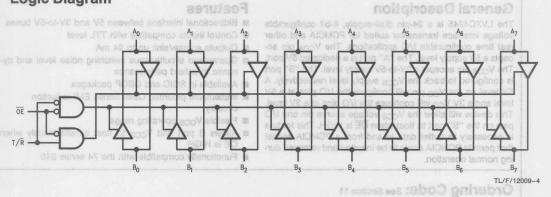
TL/F/12009-2

	SOIC JEDEC	QSOP		
Order Number	74LVXC4245WM	74LVXC4245QSC		
	74LVXC4245WMX			
See NS Package Number	M24B	MQA24		

Truth Table

	In	puts		
	EO	T/R	Outputs	POROJITESO HERRE
	L	L	Bus B Data to Bus A	74LVXC4245
	L	Н	Bus A Data to Bus B	
	HER	X	HIGH-Z State	8-Bit Dual Su
Sutputs) 9 - 1/	AIE-INT	nsceiver with	Interface Tra

Logic Diagram



Connection Diagram





Description	Pin Names
Output Enable Input	
Transmit/Receive Input	ĀVT
Side A Inputs or TRI-STATE Outputs	7A-0A
Side B Inputs or TRI-STATE Outputs	78-08

	SOIC JEDEC	
	74LVXC424SWM 74LVXC4246WMX	Order Number
MOASA	BASM	See NS Package Number

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CCA} ,V _{CCB})	-0.5V to $+7.0V$
DC Input Voltage (V _I) @ OE, T/R	-0.5V to V _{CCA} +0.5V
DC Input/Output Voltage (VI/O)	±1.0
@ An	-0.5V to V _{CCA} +0.5V
@ B _n	$-0.5V$ to $V_{CCB} + 0.5V$
DC Input Diode Current (IIK) @ OE, T	√R 0.8± ±20 mA
DC Output Diode Current (IOK)	0.8± ±50 mA
DC Output Source or Sink Current (Id	o) 0.8 ± 50 mA

DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND}) and Max Current

Storage Temperature Range (T_{STG}) DC Latch-Up Source or Sink Current

Recommended Operating

Supply Voltage V_{CCA} 4.5V to 5.5V 2.7V to 5.5V V_{CCB} 9.7V to 5.5V Input Voltage $(V_I) @ \overline{OE}, T/\overline{R}$ 0V to V_{CCA} Input/Output Voltage $(V_{I/O})$ $@A_n$ 0V to V_{CCB} B_n 0V to V_{CCB} Free Air Operating Temperature (T_A) $-40^{\circ}C$ to $+85^{\circ}C$ Minimum Input Edge Rate $(\Delta V/\Delta t)$ 8 ns/V V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3V, 4.5V, 5.5V

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

GND =	OE = GND, T/R				7	4LVXC4245			
Symbol	Parameter			V _{CCB}	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions
ADDV =	A Bn = Vocs or GN OE = GND, T/R	08		Тур	9	Guaranteed Limits	21101110		
V _{IHA}	Minimum High Level Input Voltage	A _n OE	4.5 4.5	2.7 3.6		2.0	2.0	iput 1 Oynamin	V _{OUT} ≤ 0.1V or
	(Notes 1 and 2)	T/R	5.5	5.5		2.0	2.0	V	≥ V _{CC} - 0.1V
V _{IHB}	(2 ous Lagion)		4.5	2.7		2.0	2.0	7 '	84.10
	(Notes 1 and 2)	B _n	4.5 4.5	3.6 5.5	2	2.0 3.85	20	tout Minu	OLVA Quiet Ou
V _{ILA}	Maximum Low Level Input Voltage	A _n OE T/R	4.5 4.5 5.5	2.7 3.6 5.5	8	0.8 0.8 0.8	0.8 0.8 0.8	V	V _{OUT} ≤ 0.1V or ≥ V _{CC} − 0.1V
V _{ILB}	(Notes 1 and 3)	B _n	4.5 4.5 4.5	2.7 3.6 5.5		0.8 0.8 1.65	0.8 0.8 1.65	High Le	HDA Minimun Dynamic Voltage
V _{OHA}	Minimum High Level Output Voltage		4.5 4.5	3.0 3.0	4.49 4.25	4.4 3.86	4.4	va.Lawi.lev	$I_{OUT} = -100 \text{M}$ $I_{OH} = -24 \text{m/s}$
VOHB	(Notes 1 and 3)		4.5 4.5 4.5 4.5 4.5 4.5 4.5	3.0 3.0 3.0 2.7 2.7 4.5	2.99 2.85 2.65 2.5 2.3 4.25	2.9 2.56 2.35 2.3 2.1 3.86	2.9 2.46 2.25 2.2 2.0 3.76	V actinged of outputs d	$I_{OUT} = -100 \mu$ $I_{OH} = -12 \text{mA}$ $I_{OH} = -24 \text{mA}$ $I_{OH} = -12 \text{mA}$ $I_{OH} = -24 \text{mA}$ $I_{OH} = -24 \text{mA}$ $I_{OH} = -24 \text{mA}$
Vola	Maximum Low Level Output Voltage		4.5 4.5	3.0 3.0	0.002 0.21	0.1 0.36	0.1 0.44	V	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$
V _{OLB}			4.5 4.5 4.5 4.5 4.5	3.0 3.0 2.7 2.7 4.5	0.002 0.21 0.11 0.22 0.18	0.1 0.36 0.36 0.42 0.36	0.1 0.44 0.44 0.5 0.44	v	$I_{OUT} = 100 \mu A$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$

± 50 mA

-65°C to +150°C

±200 mA

±300 mA

DC Electrical Characteristics (Continued)

				SUO	mone	74	LVXC	4245	devices a	tional	If Military/Aerospace sp please contact the Na	
Symbol	Paran	neter	V _{CCA}	V _{CCB}	T _A =	+ 25°C	TA	= -40°C	to +85°C	Units		
ADOV O	Vo	F	\T,30	(V) e	Тур	gnt (Guara	nteed Lir	The state of the s	(
I _{IN} ADDV of	Maximum Ir Leakage Cu OE, T/R		5.5 5.5	3.6 5.5	ut/Outpu An Bh	±0.1 ±0.1	±1.0 V2.0+ A(±1).01 V2.0-		μА	V _I = V _{CCA} , GND		
loza	Maximum T Output Leal		5.5 5.5	3.6 5.5	e Air Op imum Ini	±0.5 ±0.5	Am 05 ± ±5.0		μА	$V_I = V_{IL}, V_{IH}, \overline{OE} = V_{CCA}$ $V_O = V_{CCA}, GND$		
l _{OZB}	Maximum T Output Leal		5.5 5.5	3.6 5.5	/6 @ 00°	±0.5 ±0.5	Am 08 ± ±5.0 (6) ±5.0		μА	$V_I = V_{IL}, V_{IH}, \overline{OE} = V_{CCA}$ $V_O = V_{CCB}, GND$		
Δlcc	Maximum	All Inputs	5.5	5.5	1.0	1.35	Am	08± 1.5		mA	$V_I = V_{CC} - 2.1V$	
yearann	I _{CC} /Input	B _n up ad	5.5	3.6	d. The d	0.35	0.00	0.5	'aa –	mA	$V_I = V_{CCB} - 0.6V$	
ICCA1	Quiescent \ Supply Curr Port Floats		5.5	Open	onteins on are of (Recolific ontifica	8	Am 008± 80			μA	$A_n = V_{CCA}$ or GND $B_n = Open$, $\overline{OE} = V_{CCA}$ $T/\overline{R} = V_{CCA}$, $V_{CCB} = Open$	
ICCA2	Quiescent \ Supply Curr		5.5 5.5	3.6 5.5	IAN IVA	8	80 (12 ive) 80 80		μΑ	$\begin{aligned} &A_n = V_{CCA} \text{ or GND} \\ &B_n = V_{CCB} \text{ or GND} \\ &\overline{OE} = \text{GND, T/R} = \text{GND} \end{aligned}$		
ICCB	Quiescent \ Supply Curr	CCB cas	5.5 5.5	3.6 5.5	AT :	8	TAT	50 80	2.572	μΑ	$\begin{aligned} A_n &= V_{CCA} \text{ or GND} \\ B_n &= V_{CCB} \text{ or GND} \\ \overline{OE} &= GND, T/\overline{R} = V_{CCA} \end{aligned}$	
V _{OLPA}	Quiet Outpu Maximum D		5.0 5.0	3.3 5.0		1.5 1.5		2.7	4.5	A V le	(Notes 1 and 2)	
V _{OLPB}	Vol.	V	5.0 5.0	3.3 5.0		0.8		7.5	6.6 FI	٧	(Notes 1 and 2)	
V _{OLVA}	Quiet Outpu Dynamic Vo		5.0 5.0	3.3 5.0	8	-1.2 -1.2		5.6	4.5	V	(Notes 1 and 2)	
V _{OLVB}	≥ TUOV		5.0 5.0	3.3 5.0		-0.8 -1.2		3.6	4.5	o v	(Notes 1 and 2)	
V _{IHDA}	Minimum Hi Dynamic In		5.0 5.0	3.3 5.0		2.0		2.7	4.5	V	(Notes 1 and 3)	
V _{IHDB}	Voltage		5.0	3.3 5.0	8	3.5		5.5	4.5	V	(Notes 1 and 3)	
V _{ILDA}	Maximum L Dynamic Inp		5.0	3.3	8	0.8	4.25	0.8	4.6	V	(Notes 1 and 3)	
V _{ILDB}	Voltage		5.0	3.3	60 75	0.8	2.85	3.0	4.5	V	(Notes 1 and 3)	

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

				74L	/XC4245				74L	VXC	4245		100
Symbol	Parameter		V _c	CCA =	= 50 pF 4.5V to 5.5V 4.5V to 5.5V	PALVXO	C _L = 50 pF V _{CCA} = 4.5V to 5.5V V _{CCB} = 2.7V to 3.6V						Units
	AMOUNT		A = +25	°C	TA = -40°C	to +85°C	Т	A = +25	°C	TA	=	40°C to +85°C	
		Min	Typ (Note 1)	Max	Min	Max	Min	Typ (Note 2)	Max	4	Min	Max	
t _{PHL}	Propagation Delay A to B	1.0	4.9 4.0	6.5 5.5	1.0 1.0	7.0 6.0	1.0	5.5 5.0	7.5 7.0		1.0 1.0	8.0 7.5	ns
t _{PHL}	Propagation Delay B to A	1.0	4.7	6.5 5.0	1.0 1.0	7.0 5.5	1.0 1.0	5.6 4.3	7.5 6.0		1.0	8.0 6.5	ns
t _{PZL}	Output Enable Time OE to B	1.0	5.6 5.7	7.5 7.5	1.0 1.0	8.0 8.0	1.0	6.7	9.0 9.5		1.0	10.0 10.0	ns
t _{PZL} t _{PZH}	Output Enable Time OE to A	1.0 1.0	7.4 6.1	9.0 7.5	1.0 1.0	10.0 8.5	1.0	8.0	10.0		1.0 1.0	11.0 8.5	ns
t _{PHZ}	Output Disable Time OE to B	1.0	4.8	7.0 5.5	1.0 1.0	7.5 6.0	1.0	6.0 4.2	9.0		1.0 1.0	9.5 7.0	ns
t _{PHZ}	Output Disable Time OE to A	1.0 1.0	3.4 2.9	5.5 4.5	1.0 1.0	6.0 5.0	1.0	3.4 2.9	5.5 5.0		1.0	6.0 5.5	ns
toshl toslh	Output to Output Skew (Note 3) Data to Output	JZ F	1.0	1.5		1.5	0)02	1.0	1.5			1.5	ns

Note 1: Typical values at $V_{CCA} = 5V$, $V_{CCB} = 5V$ @25°C.

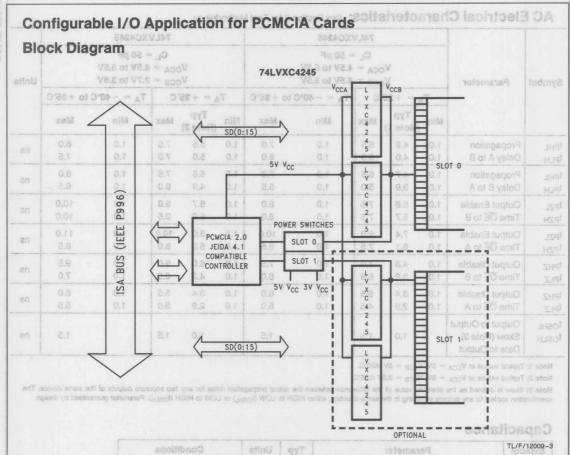
Note 2: Typical values at $V_{CCA} = 5V$, $V_{CCB} = 3.3V$ @25°C.

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance

Symbol	Parameter		Тур	Units	Conditions	
CIN	Input Capacitance	niq AGOV ei	4.5	pF	V _{CC} = Open que laub niq	The LVXC4245 is a 24
CI/O	Input/Output Capacitance	suces ues	10	pF	V _{CCA} = 5V, V _{CCB} = 3.3V	PCMCIA configurable notebook designs, the
C _{PD}	Power Dissipation Capacitance	$A \rightarrow B$	45	pF		mW of quiescent pr
LI GIN IV	(IEEE P996).	$B \rightarrow A$	50	pE	111 0011	LVXC4245 meets all F 5V and 3.3V operation

nence rail to rail output swings, maximizing the reliability of



The LVXC4245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC4245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC4245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCB} of the LVXC4245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC4245 must always be tied to a 5V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the block diagram above, the LVXC4245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).



Section 7 Contents

		nily Features	ich Fan	X Bus Swi	VJ
7-4	us-Exchange Switch	Low Power B	10-Bit	LVX3L383	74
7-7	us Switch	Low Power B	10-Bit	LVX3L384	74

Section 7 **LVX Bus Switch Family**

7



Section 7 Contents

LVX Bus Switch Family Features	7-3
74LVX3L383 10-Bit Low Power Bus-Exchange Switch	7-4
74LVX3L384 10-Bit Low Power Bus Switch	7-7

Section 7 LVX Bus Switch Family

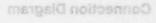


National Semiconductor

LVX Bus Switch Family Low Voltage CMOS Bus Switches

in 5Ω switch co

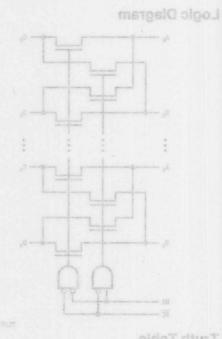
Features Aug of the rowood woll as	to a month about a Advantages to studie with dolling
State-of-the-Art sub-micron BiCMOS process	Good ESD and Latchup immunity
Quick and easy 5V to 3V translation	Allows 3.3V components to interface with 5V signals and rid-2 s
Near zero propagation delays; 250 ps typical	Facilitates high-performance bus connections and exchanges
Ultra low standby current (I _{CC} 3 μA max over temp)	Saves power, extends battery life. Ideal for portable applications
Low on resistance (Ron) and low input capacitance (Ci)	Minimizes bus loading
SOIC and QSOP	Saves board space and weight
Alternate source available	Product standardization. Ensured product supply





Description	Pin Nemes	
Bus Switch Enable		
Bus Exchange		
Buses C, D	Co-Ca, Do-Da	

	SOIC JEDEC	
		Order Number
MOA24	M248	See NS Package Number



		3100	5 1 12	11231
Penedon	B9-E4	A-oA	жа	
Disconnect				
Commeet		C ₀ -C ₄		
		D ₀ -D ₄	Ы	

Prefigiency Date: National Semiconductor reserves the right to make changes at any time without notice.

74LVX3L383 10-Bit Low Power Bus-Exchange Switch

General Description

The LVX3L383 provides two sets of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device operates as a 10-bit bus switch or a 5-bit bus exchanger. The bus exchange (BX) signal provides nibble swapping of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a quad 2-to-1 multiplexer and to create low delay barrel shifters. The bus enable (BE) signal turns the switches on.

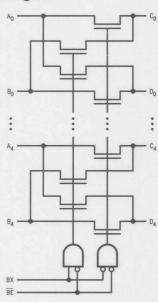
Features

- \blacksquare 5 Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 µA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC and QSOP (SSOP, 0.15" body width) packages

NOTIFICATION OF THE REAL PROPERTY OF THE PROPE

Ordering Code: See Section 11

Logic Diagram



TL/F/11652-1

Connection Diagram

Pin Assignment for SOIC and QSOP

BE - 1	0	24	_ v
$c_0 - 2$		23	— D
A ₀ - 3		22	— в
B ₀ - 4		21	— A
D ₀ - 5		20	— c
C ₁ - 6		19	— D
A ₁ - 7		18	— в
B ₁ - 8		17	— A
D ₁ — 9		16	— c
C ₂ - 1	0	15	— D
A ₂ - 1	1	14	— в
GND - 1:	2	13	—в

TL/F/11652-2

Pin Names	Description
BE	Bus Switch Enable
BX	Bus Exchange
A ₀ -A ₄ , B ₀ -B ₄	Buses A, B
C ₀ -C ₄ , D ₀ -D ₄	Buses C, D

Truth Table

BE	вх	A ₀ -A ₄	B ₀ -B ₄	Function
Н	X	High-Z State	High-Z State	Disconnect
L	L	C ₀ -C ₄	D ₀ - D ₄	Connect
L	Н	D ₀ -D ₄	C ₀ -C ₄	Exchange

	SOIC JEDEC	SSOP JEDEC
Order Number	74LVX3L383WM 74LVX3L383WMX	74LVX3L383QSC 74LVX3L383QSCX
See NS Package Number	M24B	MQA24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Supply Voltage (V _{CC}) −0.5V to +7.0V DC Switch Voltage (V _S) −0.5V to +7.0V DC Input Voltage (V _I) (Note 2) −0.5V to +7.0V	Supply Voltage (V _{CC}) Free Air Operating Temperature (T _A)		4.0V to 5.5V -40°C to +85°C
DC Input Diode Current (I_{IN}) with $V_I < 0$ — 20 mA DC Output (I_O) Sink Current 120 mA		Data Propagation Delay A ₀ to B ₀ or B ₀ to A ₀ (Note 1)	
Storage Temperature Range (T _{STG}) -65°C to +150°C Power Dissipation 0.5W	4.5	Switch Exchange Time BX to A _n or B _n	тецн триц
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The		Switch Enable Time BE to An. Bn	
parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	4.5	Switch Disenable Time BE to An. Bn	

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

DC Electrical Characteristics

				74LVX3L383	3		non) camanescac
Symbol	Parameter	Vcc	TA	= -40°C to +	85°C	Units	Conditions
o,	V _{OC} = 5.0V	(V)q	Min	Typ (Note 3)	Max	a Imput Cape Output Cape	Buen Nin
V _{IK}	Maximum Clamp Diode Voltage	4.5		8	ecnatio -1.2	Output Capa	$I_{\text{IN}} = -18 \text{mA}$
V _{IH}	Minimum High Level Input Voltage	4.0-5.5	2.0			V	
V _{IL}	Maximum Low Level Input Voltage	4.0-5.5			0.8	V	
I _{IN}	Maximum Input	0			10		$0 \le V_{IN} \le 5.5V$
	Leakage Current	5.5			±1	μΑ	
loz	Maximum TRI-STATE® I/O Leakage	5.5			±1	μΑ	$0 \le A, B \le V_{CC}$
los	Short Circuit Current	4.5	100			mA	$V_{I}(A), V_{I}(B) = 0V,$ $V_{I}(B), V_{I}(A) = 4.5V$
RON	Switch On	4.5		5	7	Ω	$V_{I} = 0V, I_{ON} = 30 \text{ mA}$
	Resistance (Note 1)	4.5		10	15	Ω	$V_{I} = 2.4V, I_{ON} = 15 \text{ m/s}$
Icc	Maximum Quiescent Supply Current	5.5		0.2	3.0	μА	$V_I = V_{CC}$, GND $I_O = 0$
ΔI _{CC}	Increase in I _{CC} per Input (Note 2)	5.5		Pal I. r	2.5	mA	V _{IN} = 3.4V, I _O = 0 Per Control Input

Note 1: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 2: Per TTL driven input ($V_{IN} = 3.4V$, control inputs only). A and B pins do not contribute to I_{CC} .

Note 3: All typical values are at $V_{CC} = 5.0V$, $T_A = 25$ °C.

AC Electrical Characteristics: See Section 2 for Test Methodology 12 F1 mumiks 14 etulo ad A

√ Symbol (.4 2°0 to +85°0	Continued of Operating College (Voorstanger (TA) Coperating Temperature (TA)	V _{CC}	74LVX3L383 T _A = -40°C to +85°C C _L = 50 pF Typ (Note 2)	ge (V _{CC})	If Military/J please cor CatinUDistr Supply Volta DC Switch V DC Input Volt
[†] PLH [†] PHL	Data Propagation Delay An to Bn or Bn to An (Note 1)	4.5	I _{IN}) with V ₁ < 0 -20 mA ant 120 mA		DC Input Did DC 80 Iput (I)
t _{PLH}	Switch Exchange Time BX to A _n or B _n	4.5	W8.01.5	6.5 noite	Storage Len
t _{PZL}	Switch Enable Time BE to A _n , B _n	4.5	wommen names are base values y of the device cannot be 13 yearsh not be operated at these limits. The	6.5	pidw basyed
t _{PLZ}	Switch Disenable Time BE to A _n , B _n	4.5	d in the "Electrical Characteristics" d at the absolute maximun 2.1 tings, sention Conditions" table will define	5.5	on evens det

Note 1: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Note 2: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

Capacitance (Note)

	Symbol		Paramete	er age	Тур	Max	Units	Conditions	
Г	CIN	Contro	ol Input Cap	pacitance	4		pF	V _{CC} = 5.0V	Symbol
	C _{I/O} (ON) Input/	Output Cap	pacitance	(8.81014)	niiñ	pF	V _{CC} = 5.0V		
	C _{I/O} (OFF)	Input/	Output Cap	pacitance	6		pF	V _{CC} = 5.0V _C mumixsM	
No	te: Capacitance is c	haracterize	d but not test	ed.			6,5	Diode Voltage	
						2,0	4.0-5.5	Minimum High Level Input Voltage	
								Maximum Low Level Input Voltage	VII.V
	Vä.ā≥ _W						0	Maximum Input	Nig
							6.5	Leakage Current	
			Au	1±				Maximum TRI-STATE®	
								Short Circuit Current	
	N, ION = 30 m/	V ₁ == (
	2.4V, lon = 15 r	\ = V					PF V _{CC} = 5. O.S d.d-O.A egal d.d-O.A egal d.d-O.A form d.d d.d form d.d form d.a (finite	Resistance (Note 1)	
								Maximum Quiescent	

lets it Measured by voltage drop between A and B pin at indicated current thirough the switch. On resistance is defermined by the lower of the voltages on the two

Note 2: Per TTL driven input (Vin = 3.4V, control inputs only). A and B pins do not contribute to Icc

Veta 3: At typical values are at Von = 5.0V. Ta = 28°C.

DC Electrical Characteristics



74LVX3L384 10-Bit Low Power Bus Switch

General Description

The LVX3L384 provides 10 bits of high-speed CMOS TTL-compatible bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The device is organized as two 5-bit switches with separate bus enable ($\overline{\text{BE}}$) signals. When $\overline{\text{BE}}$ is low, the switch is on and port A is connected to port B. When $\overline{\text{BE}}$ is high, the switch is open and a high-impedance state exists between the two ports.

Features

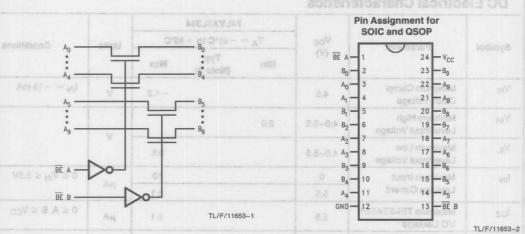
- \blacksquare 5 Ω switch connection between two ports
- Zero propagation delay
- Ultra low power with 0.2 µA typical I_{CC}
- Zero ground bounce in flow-through mode
- Control inputs compatible with TTL level
- Available in SOIC and QSOP (SSOP 0.15" Body width)

If Willtary/Aercapase specified devices are required, please contact. the National Semiconductor Sales Office/Districtors for availability and apecifications.

Ordering Code: See Section 11

Logic Diagram

Connection Diagram



Truth Table

BE A	BE B	B ₀ -B ₄	B ₅ -B ₉	Function
L	AL.	A ₀ -A ₄	A ₅ -A ₉	Connect
L	Н	A ₀ -A ₄	HIGH-Z State	Connect
Н	F =	HIGH-Z State	A ₅ -A ₉	Connect
H	Н	HIGH-Z State	HIGH-Z State	Disconnect
		11 0 000	100.00	

Pin Names	Description
 BE A, BE B	Bus Switch Enable
A ₀ -A ₉	Bus A
B ₀ -B ₉	Bus B

	SOIC JEDEC	SSOP JEDEC
Order Number	74LVX3L384WM	74LVX3L384QSC
	74LVX3L384WMX	74LVX3L384QSCX
See NS Package Number	M24B	MQA24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0VSupply Voltage (VCC) -0.5 to +7.0V DC Switch Voltage (VS) -0.5 to +7.0V DC Input Input Voltage (V_I) (Note 2) DC Input Diode Current with (V_I < 0) -20 mA DC Output (IO) Sink Current 120 mA

Storage Temperature Range (TSTG) -65°C to +150°C **Power Dissipation** valeb noitenagong one 0.5W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaran- bound landlibes polisiened to valob not spegging polibes teed. The device should not be operated at these limits. The send live field out as been ago at each of a select actual. parametric values defined in the "Electrical Characteristics" of the sale and standard characteristics. table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define easier of the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Connection Diagram

Recommended Operating Conditions

10-Bit Low Power Bus Switch

Supply Voltage (Vcc) Free Air Operating Temperature (TA)

4.0V to 5.5V -40°C to +85°C

DC Electrical Characteristics

	Pin Assignment for SOIC and QSOP		74LVX3L3	384			
Symbol	Parameter	Vcc	$T_A = -40^{\circ}C$ to	+85°C	Units	Conditions	
Oymbo.	24 - V _{CC}	A 36 (V)	Min Typ (Note 3	Max			
V _{IK}	Maximum Clamp Diode Voltage	4.5	di _s	-1.2	V	$I_{\text{IN}} = -18 \text{mA}$	
V _{IH}	Minimum High Level Input Voltage	4.0-5.5	2.0		V		
V _{IL}	Maximum Low Level Input Voltage	4.0-5.5		0.8	ľ		
I _{IN}	Maximum Input	8 0		10		0 ≤ V _{IN} ≤ 5.5V	
	Leakage Current	5.5		±100	μΑ	g 18	
IOZ	Maximum TRI-STATE®	5.5	TL/F/11853-1	±1	μА	0 ≤ A, B ≤ V _{CC}	
los	Short Circuit Current	4.5	100		mA	$V_{I}(A), V_{I}(B) = 0V,$ $V_{I}(B), V_{I}(A) = 4.5V$	
Ron	Switch On	4.5	nolloni 5	ed-7	Ω	$V_{I} = 0V, I_{ON} = 30 \text{ mA}$	
eldan	Resistance (Note 1)	BEA, BEB	1001110	15 A	Ω MA	$V_1 = 2.4V, I_{ON} = 15 \text{ mA}$	
Icc	Maximum Quiescent Supply Current	5.5 5.5	toenn 0,2	3.0. ₈ A	μΑ	$V_1 = V_{CC}$, GND $I_0 = 0$	
ΔICC	Increase in I _{CC} per Input (Note 2)	5.5	Disconnect	2.5	mA	V _{IN} = 3.4V, I _O = 0 Per Control Input	

Note 1: Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two

Note 2: Per TTL driven Input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to Icc. Note 3: All typical values are at V_{CC} = 5.0V, T_A = 25°C.

Preliminary Date: National Semiconductor reserves the right to make changes at any time without notice.

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AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVX3L384		
Symbol	Parameter	V _{CC} (V)	T,	$C_L = -40^{\circ}C \text{ to } + 85^{\circ}C$	5°C	Units
			Min	Typ (Note 2)	Max	
T _{PLH} T _{PHL}	Data Propagation Delay An to Bn or Bn to An (Note 1)	4.5			0.25	ns
T _{PZL} T _{PZH}	Switch Enable Time BE _A , BE _B to An, Bn	4.5	1.5		6.5	ns
T _{PLZ} T _{PHZ}	Switch Disable Time BE _A , BE _B to An, Bn	4.5	1.5		5.5	ns

Note 1: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the load capacitance. The time constant for the switch and alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Note 2: All typical values are at $V_{CC} = 5.0V$, $T_A = 25$ °C.

Capacitance (Note)

Symbol	Parameter	Тур	Max	Units	Conditions
C _{IN}	Control Input Capacitance	4		pF	$V_{CC} = 5.0V$
C _{I/O} (ON)	Input/Output Capacitance	8		pF	$V_{CC} = 5.0V$
C _{I/O} (OFF)	Input/Output Capacitance	6		pF	V _{CC} = 5.0V

Note: Capacitance is characterized but not tested.

	$C_L = 80 \mathrm{pF}$			-(V)	19/07/10/20 3	constitute.
	xeM	Typ (Note 2)	Min			
ns	0.25			4.5	Data Propagation Delay An to Bn or Bn to An (Note 1)	
	8.6		1.5	4,5	Switch Enable Time BE _A , BE _B to An, Bn	ТРZL ТРZН
	5.5			4.5	Switch Disable Time BEA, BE _B to An, Sn	TPLZ TPHZ

Note it. This parameter is guaranteed by design but not tested. The bus awitch contributes no propagation delay other than the RC delay of the On resistance of the switch and sional to the awitch and sional to the propagation delay of the switch and sional to the system. Propagation delay of the bos switch when used in a system is than the day the driving signals, it adds very title propagation delay to the system. Propagation delay of the bos switch when used in a system is detarmined by the driving choic or the driving side of the switch and its interaction with the load on the driven eds.

Note 2: All typical values are at $V_{\rm CC} = 5.0 \rm V$, $T_{\rm A} = 25^{\circ} \rm C$.

Capacitance (Note)

Symbol	Porameter	Typ	xsW	Units	Conditions
CIN	Control Input Capacitance	4			$V_{CC} = 5.0V$
G _{I/O} (ON)	Input/Output Capacitance	8			$V_{CC} = 5.0V$
	Input/Output Capacitance	3			$V_{\rm GC} = 5.0V$

Note: Capacitance is characterized but not tested.



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8-16	74LVX14 Low Voltage Hex Inverter with Schmitt Trigger Input
8-19	74LVX32 Low Voltage Quad 2-Input OR Gate
8-22	74LVX74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop
8-26	74LVX86 Low Voltage Quad 2-8 noitoeSOR Gate 74LVX125 Low Voltage Quad Burner with 1MI-STATE Outputs.
8-29	74LVX125 Low Voltage Quad Burner with 1 MI-STATE Outputs.
8-32	74LVX138 Low Voltage 1-cylima XVultiplexer
	74LVX138 Low Voltage 1-vilame XVultiplexer 74LVX157 Low Voltage Quad 2-Input Multiplexer
	74LVX174 Low Voltage Hex D Flip-Flop with Master Reset
	74LVX240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
8-46	74LVX244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
8-49	74LVX245 Low Voltage Octal Bidirectional Transceiver
8-52	74LVX273 Low Voltage Octal D Flip-Flop
8-56	74LVX373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs
	74LVX374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs
	741 VX5731 ow Voltage Octal Latch with TRLSTATE Outputs



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General Description

74LVX00

LVX Family Low Voltage CMOS Logic (with 5V tolerent inputs)

The LVX00 contains four 2-input NAND gates. The inputs tolerate voltage level translation from 5V to 3V tolerate voltages up to 7V allowing the interface of 5V sys-

Features	Advantages
Extended V_{CC} range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation
0.8 μm CMOS process	High performance with propagation delays as fast as 7.0 ns max for octals
No Input-diode clamp to VCC 10 1000000000	Interfaces directly to industry standard buses and 5V systems at inputs
Low standby current (I _{CC} 40 µA max for octal over temp)	Saves power, extends battery life
±4 mA drive current	Balanced drive
SOIC, EIAJ-SOIC and SSOP I packaging	Saves board space and weight; TSSOP compatible with PCMCIA standards
Alternate source available	Product standardization. Ensured product supply

Description	Pln Names
inputs	An Bn
Oatputs	00

SSOP TYPE I	SOIC EIAJ	23031 2108	
74LVX00MSCX	74LVX00SJ 74LVX00SJX	74LVX00M 74LVX00MX	Order Number
MSC14	MIND	M14A	See NS Package Number





74LVX00 Low Voltage Quad 2-Input NAND Gate

General Description

The LVX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

IEEE/IEC

(ajugni ine Features filiw)

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and noise recognition of the state of the state

Ordering Code: See Section 11 Million someones dell'A

Logic Symbol and brahasty standard to tribonic securiorists

FIONNIN POMOIA

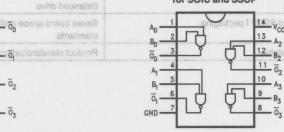
Bo .

B₁ = A₂ = A₃ =

B₃

Connection Diagram and eholb-fud

(gras) nevo Pin Assignment (# 00) Inemus ydbrasi for SOIC and SSOP



TL/F/11551-3

Saves power, extends battery life

TL/F/11551-2

Pin Names	Description
A _n , B _n	Inputs
Ōn	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX00M 74LVX00MX	74LVX00SJ 74LVX00SJX	74LVX00MSCX
See NS Package Number	M14A	M14D	MSC14

Recommended Operating 10 981014 Absolute Maximum Ratings (Note) If Military/Aerospace specified devices are required, **Conditions** please contact the National Semiconductor Sales Supply Voltage (V_{CC}) 2.0V to 3.6V Office/Distributors for availability and specifications. 0V to 5.5V Input Voltage (V_I) Supply Voltage (VCC) -0.5V to +7.0VOutput Voltage (VO) OV to VCC DC Input Diode Current (I_{IK}) Operating Temperature (T_A) -40°C to +85°C $V_1 = -0.5V$ -20 mA Input Rise and Fall Time (Δ_t/Δ_v) 0 ns/V to 100 ns/V DC Input Voltage (V_I) -0.5V to 7V DC Output Diode Current (IOK) $V_0 = -0.5V$ -20 mA Maximum Low Level Dynamic Input Voltage $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (Vo) -0.5V to $V_{CC} + 0.5V$ DC Output Source AC Electrical Characteristics: See Section 2 to Am 25 # Incidology or Sink Current (IO) DC V_{CC} or Ground Current ±50 mA (ICC or IGND) Storage Temperature (TSTG) -65°C to +150°C 48°C to +85 Power Dissipation 180 mW Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter			74LVX0)	langt-out 7	4LVX	00	ugt = HJ	guaranteed by dealign to	Note 1: Parameter
		Vcc	T _A = +25°C			T _A = -40°C to +85°C			Units	Conditions SQSQ	
			Min	Тур	Max	Min	0	Max			
V _{IH}	High Level Input	2.0	1.5 2.0	85°C	TA =	1.5		$T_{A} = +2i$	٧	Parameter	Symbol
	Voltage	3.6	2.4	xel	VE.	2.4		gyT :	ning		
V _{IL}	Low Level	2.0	g	01	0.5		01	0.5	V	Input Capacitance	
Voltage	3.6	q		0.8			0.8		Power Dissipation	CPD	
V _{OH}	High Level Output Voltage	2.0 3.0	1.9 2.9	2.0	ent mon		döirliw eo	nefosgso fnet	sviuto <mark>v</mark> emi	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$
	voltage	3.0	2.58		col	2.48	X 1992	7.11.30000 THE	Supe ent W	PRINTERS IN 1972 THE STREET	$I_{OH} = -4 \text{ mA}$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36	(per Sate)		0.1 0.1 0.44	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$
I _{IN}	Input Leakage Current	3.6			±0.1			±1.0	μА	V _{IN} = 5.5V or GND	
Icc	Quiescent Supply Current	3.6		r	2.0	20.0 μ A $V_{IN} = V_{CC}$ or GND)		

8

	177 - 19-		Condit		re requ	Anna La Tomas	74	LVX00	y/Aerospace	if Milital
Symbol	2.0	Paramet	Supply Vot	ACC.		A CC				C _L (pl
IV to 5.5V			Input Volta	-0.5V to +7.0V			Typ Limit		nito(V) egatio	Supply V
VOLP +	Quiet Output Maximum D	ynamic V _{OL}	Operating	Am 0	C-	3.3	0.3	(2111)	5 Van	50
VOLV OO!	Quiet Output Minimum Dy	namic V _{OL}	Input Rise	V7 o	-0.5V	3.3	-0.3	-0	0.5 V ap VioV	Juga 50
V _{IHD}	Minimum High Level Dyna	amic Input Vo	oltage			3.3	1	(OI) 12	at Dyode Curo	du050
VILD	Maximum Low Level Dyn	amic Input Vo	oltage	Am 0		3.3		0	.8 V V V	50
	t _r = t _f = 3 ns) ectrical Charact	eristics:	See Secti		t Method	lology		form	ut Voltage (Vo ut Source Current (Io)	OC Outp or Sink
				74LVX00	3.6	7	4LVX00	rent		10 001)
Symbol	Parameter	V _{CC} (V)		A = +25°C	130	~80 -40	T _A = (ana T) and 0°C to +85°C			C _L (pl
			Min	Typ seul	the second		m Ratin			Vote: 7/h
t _{PLH} , t _{PHL}	Propagation Delay Time	2.7		- Fine	es firmits	1.0	Asnoqė e	d not b	e device si reul	15
PAL			-	4.1 6.2		0.1			ic values defin	tem 50
		3.3 ±0.3	-			1.0 lulos		Desert	commended t	15
	0 0					noi1.0 q			conditions for	ent 50
toslh, toshl	Output to Output Skew (Note 1)	2.7			.5	ristic	acte	15.50	leo nso	50
Symbo	I Parameter	74LVX00		1.5	74LVX0	Тур 0	Min Typ		High Level	Н
Symbo	Parameter	Min	= +25°C	ax SMin	°C to +	85°C	2.0	0.8	Input Voltage	
	Input Capacitance		20.00	0	8.0		pF	2,0	Low Level	
CINI		V	8.0 9		8.0			3.0	Input Voltage	
C _{IN}	Power Dissipation Capacitance (Note 1)	-				2.0	urrent con	sumption	High Level Output	HO
CPD Note 1: CPD without load	Capacitance (Note 1) is defined as the value of the inter	rnal equivalent ca		0.5		pperating ci	2.58	3.0	Voltage	
CPD Note 1: CPD without load	Capacitance (Note 1) is defined as the value of the interrating current can be obtained by	rnal equivalent carrier the equation: Id		ich is calculated × V _{CC} × f _{IN} + 4 (per Gate)		0.0	0.3	0.0	Voltage Cutput Voltage	JC
CPD Note 1: CPD without load Average ope	Capacitance (Note 1) is defined as the value of the interrating current can be obtained by	rnal equivalent carries of the equation: It	$CC(opr.) = \frac{C_{PD}}{CC(opr.)}$	\times V _{CC} \times f _{IN} +	1.0 1.0	0.0	0.3	0.0 0.0 2.0 3.0	Low Level Output	
Note 1: C _{PD} without load Average ope	Capacitance (Note 1) is defined as the value of the interpracting current can be obtained by	rnal equivalent co	$CC(opr.) = \frac{C_{PD}}{CC(opr.)}$	\times V _{CC} \times f _{IN} +	1.0 1.0 1.0 0.38	0.0	0.3	3.0 2.0 3.0 3.0	Low Level Output Voltage Input Leakage) (a)

Output Voltage (Vo) 74LVX02 Low Voltage Quad 2-Input NOR Gate

General Description

The LVX02 contains four 2-input NOR gates. The inputs A Input voltage level translation from 5V to 3V tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP pack-

Absolute Maximum Ratings (Note) If Military/Aerospece specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Input Diode Current (Isc)

Storage Temperature (Tsrg)

Power Dissipation

 $V_1 = -0.5V$ DC Input Voltage (V_I)

■ Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbol

Note: The "Absolute Maximum Patinus" are those values Connection Diagram as ed doing broyed

apriliar mumbrain etulo Pin Assignmentaraup ton era eldat IEEE/IEC on the billion and same for SOIC and SSOP · 00 13 02 B₀ -B₂ B - A2 = AT anolilbncA2 10 03 0238+01000-B₂ 9 B A3 . GND B₃ -TL/F/11600-2 TL/F/11600-1 BV 8.0 Au 08- = HO! Au 03 - = HO **Pin Names** Description lot = 50 MA An, Bn Inputs 0.0 Low Level lot = 20 HV On I. Outputs lot = 4 mA Current

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX02M	74LVX02SJ	
	74LVX02MX	74LVX02SJX	74LVX02MSCX
See NS Package Number	M14A	M14D	MSC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})

-0.5V to +7.0V

DC Input Diode Current (IIK) $V_1 = -0.5V$

-20 mA

DC Input Voltage (VI)

-0.5V to 7V

DC Output Diode Current (IOK) $V_0 = -0.5V$

-20 mA

DC Output Voltage (Vo) -0.5V to V_{CC} + 0.5V

DC Output Source

a Available in SOIC JEDEC, SOI

or Sink Current (IO) DC V_{CC} or Ground Current ±25 mA

(ICC or IGND)

±50 mA

Storage Temperature (TSTG)

-65°C to +150°C

Power Dissipation

180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC})

2.0V to 3.6V

Input Voltage (V_I)

0V to 5.5V

Output Voltage (VO)

OV to Vcc

Operating Temperature (TA) Input Rise and Fall Time (Δ_t/Δ_v)

-40°C to +85°C 0 ns/V to 100 ns/V

General Description

Logic Symbol

DC Electrical Characteristics

Symbol	Parameter	7		74LVX0)2	74	LVX02		3		
		Vcc	T	= +2	5°C		T _A = -40°C to +85°C		Conditions		
	E8 - 8 L	9	Min	Тур	Max	Min	Max		Ag record		
VIH	High Level	2.0	1.5	Thirth-		1.5	80		B3		
1./F/11600-1	Input Voltage	3.0 3.6	2.0 2.4			2.0		V			
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V			
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0	Dasc	1.9 2.9 2.48	Pin Names	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$	
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$	
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μΑ	V _{IN} = 5.5V or GND		
Icc	Quiescent Supply Current	3.6			2.0		20.0	μΑ	V _{IN} = V _{CC} or GN	D	

SEOP TYPE I			
74LVXG2MSCX	74LVX02SJ 74LVX02SJX		Order Number
MSC14		M14A	See NS Package Number

lenoHel/RS

Noise Characteristics: See Section 2 for Test Methodology

			74L	VX02	nooin	
Symbol	Parameter	V _{CC}	T _A =	25°C	Units	Conditions C _L (pF)
		(*)	Тур	Limit	M	TAI VXI
VOLP	Quiet Output Maximum Dynamic VOL	3.3	0.3	0.5	V	50
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.3	-0.5	V	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
VILD	Maximum Low Level Dynamic Input Voltage	3.3	The inni	0.8	Via Viate	50

ages up to 7V allowing the interface of 5V systems to 3V a lideal for low power/low noise 3.3V appliance of 5V systems to 3V available in SOIC JEDEC, SOIC EIAJ and SSOP

AC Electrical Characteristics: See Section 2 for Test Methodology

	mance	neshold perfo	Nomamic (LVX0	2	7	4LVX02		
Symbol	Parameter	V _{CC} (V)	T _A =	+ 25	°C		T _A = C to +85°C	Units	C _L
			Min	Тур	Max	Min	Max		
t _{PLH} ,	Propagation Delay Time	2.7	connec	5.9	10.7	1.0	13.5	s Symi	15
tPHL				8.4	14.2	1.0	17.0		50
	ssignment C and SSOP	33403		4.5	6.6	1.0	0.8 8/180	ns	15
		3.3 ±0.3		7.0	10.1	-1.0	11.5		50
toshh	Output to Output Skew (Note 1)	2.7			1.5	p d	1.5	ns	50

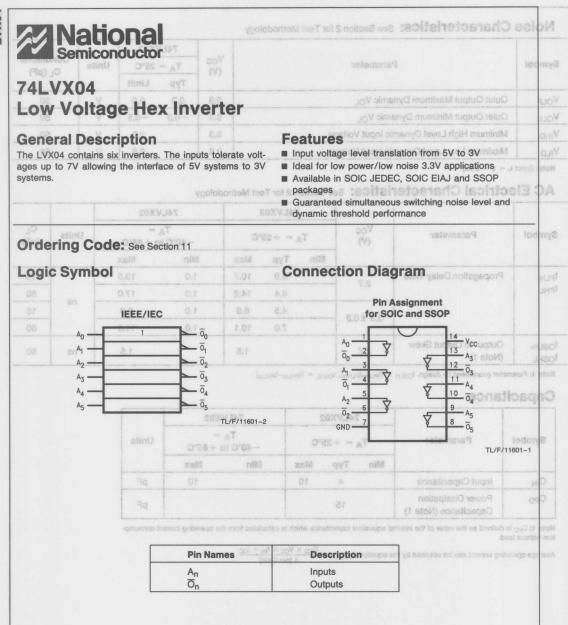
Note 1: Parameter guaranteed by design. tosh = |tphmtphm|, tosh = |tphmtphm|

Capacitance -

	8 8	1	74LVX0	2	S-roar74L	/X02	CHOICE C JOSCOCO
Symbol	Parameter	т,	A = +25	5°C		= o +85°C	Units
		Min	Тур	Max	Min	Max	
CIN	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 1)		15				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$



	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX04M 74LVX04MX	74LVX04SJ 74LVX04SJX	74LVX04MSCX
See NS Package Number	M14A	M14D	MSC14

If Military/Aerospace specified of please contact the National S Office/Distributors for availability	emicono and spe	ductor Sales ecifications.	Supply	ditions Voltage (V _{CC}) oltage (V _I)		.0V to 3.6V 0V to 5.5V
Supply Voltage (V _{CC})	-(0.5V to +7.0V		Voltage (V _O)		OV to V _{CC}
DC Input Diode Current (I_{IK}) $V_I = -0.5V$		-20 mA		ng Temperatu	re (T _A)	
DC Input Voltage (V _I)	8.8	-0.5V to 7V	Input R	ise and Fall Tir	me (Δ_t/Δ_v) 0 ns/V to	100 ns/\
DC Output Diode Current (IOK)	8.8		91	ric Input Voltage	Minimum High Level Dynan	
$V_{O} = -0.5V$ $V_{O} = V_{CC} + 0.5V$	8.3	-20 mA +20 mA	96	nic Input Voltag	Maximum Low Level Dynan	0.1
DC Output Source or Sink Current (I _O)		to V _{CC} + 0.5V	ee Section	e :golfalt	ctrical Character	AC Ele
DC V _{CC} or Ground Current		±50 mA	cienco - con onco -			
Storage Temperature (T _{STG}) Power Dissipation	-65 0 04-	5°C to +150°C 180 mW	T _A =	V _{CC} (V)	Parnmoter	lodeny
Note: The "Absolute Maximum Rational Property of the Control of th			T niM			
beyond which the safety of the deviced. The device should not be operaparametric values defined in the "Ele	ated at the	ese limits. The		2.7	Propagation Delay Time	
table are not guaranteed at the absorber "Recommended Operating Cond	ditions" ta			8,9 ± 0,3		
the conditions for actual device open	lauon.	1 1750 1011				

				74LVX	04	In a set must	74LV	X04	ugil = iteu	of ingless yd bestrungug	
Symbol	Parameter	Vcc	Т,	A = +2	25°C	-40	T _A	= + 85°C	Units	Condi	Capacenoit
			Min	Тур	Max	Min		Max			
V _{IH}	High Level Input	2.0	1.5 2.0		TA = 40°C to =	1.5 2.0	1	TA = +25°C	٧	Perameter	Symbol
	Voltage	3.6	2.4	xaM	81	2.4	veld	Typ	250.5		
VIL	Low Level	2.0		10	0.5			0,5	V	nput Capacitance	CIN
	Voltage	3.6			0.8			0.8		Power Dissipation	Gpp I
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0	at from the	1.9 2.9 2.48		alent uppackano	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \mu A$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36	(edsil) req	3	0.1 0.1 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 \text{ mA}$
I _{IN}	Input Leakage Current	3.6			±0.1			±1.0	μΑ	V _{IN} = 5.5V or GN	D
Icc	Quiescent Supply Current	3.6			2.0			20.0	μА	$V_{IN} = V_{CC}$ or GNI)

100 0			OUTIDA			require or Salo	Assert Supposed Supposed	74	LVX04	edit to	y/Aer conta	oloase
Symbol		Param	eter	Suppl			VCC	VI TA	= 25°C		Inits	C _L (pF
anV at VD			t Veltag		V(10 + 7,0	V8.0-	Тур	Lin	nit V	oltage	Supply V
V _{OLP}	Quiet Output Maximum Dy	ynamic V _O	neT goit	SteqO	Ar	n 0s	3.3	0.3	0.	5	V _{a.0}	50
V _{OLV} 00	Quiet Output Minimum Dy	namic V _{OI}	ns saif	Input	V	0.5V to	3.3	-0.3	-(0.5(\) eg	VolV	nugr 500
V _{IHD}	Minimum High Level Dyna	mic Input	Voltage	9		100	3.3	(2. (lok	o und eb	V	50
V _{ILD}	Maximum Low Level Dyna	amic Input	Voltage	Э		n 03 +	3.3		0.	8 Va.0	V	50
	t, = t _f = 3 ns) ectrical Characte	eristic	S: See	e Section :			nodology		(eon	ut Sou	OC Outpi OC Outpi or Sinic
				74L	VX04	× 02 ×	74	4LVX04	rent	und Gui	or Gro lawo)	10 00l)
Symbol	Parameter	V _{CC}		T _A =	+ 25°	0 + 160 180 m		T _A = C to +	85°C	0	nits	C _L (pl
				Min T	ур 😁	Max	gs niM re tho	m Ratii	Max		dA" e	Vote: Th
t _{PLH} ,	Propagation Delay Time	2.7			5.4	10.1	1.0	idelp eu	12.5	ine seru re st rout	vnich devic	15
		1		-	70	100	0.10	ela" er	100	and dollar	de valu	
t _{PHL}					7.9	13.6	B IIBNO ITO ITO	Sodo N	16.0			50
[†] PHL		3.3 ±0	0.3		4.1	6.2	1.0	e abso g Cand	7.5		ns	15
[†] PHL		3.3 ±0	0.3	4	98	Unided tra	www.mm ond	e abso g Cand e opera	41 15 too	uarantee ende <u>ed C</u>		one elife
^t OSLH, ^t OSHL Note 1: Para	Output to Output Skew (Note 1) Imeter guaranteed by design. tost	2.7	-t _{PLHn} , t	OSHL = tp _H	4.1 6.6	9.7 1.5	1.0	e abso g Cond (acte	7.5	uarantee ended <u>C</u> for ectua	ns anoti	15
^t OSLH, ^t OSHL Note 1: Para	(Note 1)	2.7	-t _{PLHn} , t	OSHL = tp	4.1 6.6	6.2 9.7 1.5	1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0	e abso g Cond (acte	7.5 11.0 1.5	viaramen ended C for actual	ns anoti	15 50 50
^t OSLH, ^t OSHL Note 1: Para	(Note 1) Imeter guaranteed by design. tost	2.7	74LVX	04 04	4.1 6.6	6.2 9.7 1.5	0.1 20	e absolute of the control of the con	7.5 11.0 1,5	uara mesa mesa chu achu achu achu achu achu achu achu	ns on a minor of the state of t	15 50 50
toslh, toshl Note 1: Para	(Note 1) Imeter guaranteed by design. tosi Itance Parameter	2.7	74LVX Typ	OSHL = Itp	4.1 6.6	6.2 9.7 1.5 74I T -40°C	1.0 1.0 2011a14 2011a1	e absolute of the control of the con	7.5 11.0 1.5 Jnits	variante of control of	ns on minor and in the control of th	15 50 50
toshh. Note 1: Para Capac Symbol	(Note 1) Imeter guaranteed by design. tost Itance Parameter Input Capacitance	2.7	74LVX	04 04	4.1 6.6	6.2 9.7 1.5	1.0 1.0 2011314 40XVJ4V 0°3S+ = A LVX04 (A = to +85°C Max	e absolute of the control of the con	7.5 11.0 1,5	ware meeter for action of the column of the	Para High Volta Input Low	15 50 50
toslh, toshl Note 1: Para Capac	(Note 1) Imeter guaranteed by design. tost Itance Parameter Input Capacitance Power Dissipation	2.7	74LVX Typ	OSHL = Itp	4.1 6.6	6.2 9.7 1.5 74I T -40°C	1.0 1.0 1.0 2.0112114 2.011214	e absolute of the control of the con	7.5 11.0 1.5 Jnits	ware meeter for action of the column of the	ns some some Para Para Purph High Volta	15 50 50
toshh. Note 1: Para Capac Symbol Cin CpD	(Note 1) Imeter guaranteed by design. tost Imput Capacitance Power Dissipation Capacitance (Note 1)	2.7 H = tpuhm	74LVX 74LVX 1A = +2 Typ 4	00000000000000000000000000000000000000	4.1 5.6 HLm-tpH	6.2 9.7 1.5 74I T -40°C	1.0 1.0 1.0 2.011.2114 2.01114 2.0114 2.0114 2.0114 2.0114 2.0114 2.0114 2.0114 2.0114 2.0114 2.0114 2.0114 2.	a chard of c	7.5 11.0 1.5 Jnits pF	tuere ribes of control of the contro	ns on minor is another in the input Low	15 50 50
Capac Symbol Cin Cpp Note 1: Cpp Note 1: Cpp Tion without I	(Note 1) Imeter guaranteed by design. tost Itance Parameter Input Capacitance Power Dissipation Capacitance (Note 1) is defined as the value of the integral	2.7 LH = tpLHm	74LVX Typ 4 18	04 25°C Max 10	4.1 4.1 5.6.6 in is calculated and its calculated a	6.2 9.7 1.5 74II — 40°C Min	1.0 1.0 1.0 1.0 2.11214 2.21224 2.2224	a chard of c	7.5 11.0 1.5 Jnits pF	uard nise of control of the control	ns on more and a more	15 50 50
Capac Symbol Cin CpD Note 1: CpD Note 1: CpD Average ope	(Note 1) Imeter guaranteed by design. tost Itance Parameter Input Capacitance Power Dissipation Capacitance (Note 1) is defined as the value of the integral. Parameter	2.7 LH = tpLHm	74LVX Typ 4 18	OSHL = tp) O4 25°C Max 10	4.1 4.1 5.6.6 in is calculated and is calculated as a calculat	6.2 9.7 1.5 1.5 74I T -40°C Min	1.0 1.0 1.0 1.0 2.1 2.1 2.1 2.1	or current c	7.5 11.0 1.5 Jnits pF pF	uard nise of control of the control	no en	15 50 50
Capac Symbol Cin CpD Note 1: CpD Note 1: CpD Average ope	(Note 1) Imeter guaranteed by design. tost Itance Parameter Input Capacitance Power Dissipation Capacitance (Note 1) is defined as the value of the integral. Parameter	2.7 LH = tpLHm	74LVX 74LVX 74LVX 18 18 18 18 18 10 10 10 10 10	OSHL = tp) O4 25°C Max 10	4.1 5.6 HLm-tpH	6.2 9.7 1.5 74I T -40°C Min	1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0	or current c	7.5 11.0 1.5 Jnits pF onsump	Level	no en	15 50 150 10dmy
Capac Symbol Cin Cpp Note 1: Cpp tion without I	(Note 1) Immeter guaranteed by design. tost itance Parameter Input Capacitance Power Dissipation Capacitance (Note 1) is defined as the value of the interest oad.	2.7 H = tpLHm:	74LVX 74LVX Typ 4 18 ent capac	OSHL = tp) O4 25°C Max 10	4.1 5.6 HLm-tpH	6.2 9.7 1.5 74II -40°C Min	1.0 1.0 1.0 1.0 2.11	or current c	7.5 11.0 1.5 Jnits PF PF Onsump-	Level	no en	15 50 10dmy
Capac Symbol Cin Cpp Note 1: Cpp tion without I	(Note 1) Imeter guaranteed by design. tost Itance Parameter Input Capacitance Power Dissipation Capacitance (Note 1) is defined as the value of the integral. Parameter	2.7 H = tpLHm:	74LVX 74LVX 74LVX 18 18 18 18 18 10 10 10 10 10	OSHL = tp) O4 25°C Max 10	4.1 5.6 HLm-tpH	6.2 9.7 1.5 74I T -40°C Min	1.0 1.0 1.0 1.0 2.11	or current c	7.5 11.0 1.5 Jnits pF onsump	Level	no en	15 50 50 H

Output Voltage (Vo) 74LVX08 **Low Voltage Quad 2-Input AND Gate**

General Description

The LVX08 contains four 2-input AND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

IEEE/IEC

Features

- Input voltage level translation from 5V to 3V = ○V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Storage Temperature (Targ)

13 A20813 00

Jugn TL/F/11602-1

12 B₂

1102

10 A3

9 B₃

8 03

Absolute Maximum Ratings (Note) If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales

Ordering Code: See Section 11

Logic Symbol

Ag 08

lot = 20 my

lot = 4 my

Connection Diagram

Pin Assignment for SOIC and SSOP

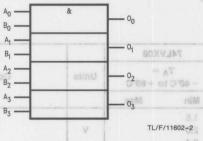
teed. The device should not be operated at those limits. The

Bo

00

GND-

6.1



A_n, B_n

On

Pin Names Description Inputs Outputs

SOIC JEDEC SOIC EIAJ SSOP TYPE I Order Number 74LVX08M 74LVX08SJ 74LVX08MX 74LVX08SJX 74LVX08MSCX See NS M14A M14D MSC14 Package Number

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})

-0.5V to +7.0V

DC Input Diode Current (IIK) $V_1 = -0.5V$

-20 mA

DC Input Voltage (VI)

0.5V to 7V

DC Output Diode Current (IOK) $V_0 = -0.5V$

-20 mA

DC Output Voltage (Vo) exion wol/19-0.5V to Vcc + 0.5V ametays Vc to each entire the private VT of our segation entire voltage.

DC Output Source A SOLO E SOLO E No and eldslisvA or Sink Current (IO)

25 mA

DC V_{CC} or Ground Current

eonamiched bloriserit oin 50 mA

(ICC or IGND) Storage Temperature (TSTG)

-65°C to +150°C

Power Dissipation

180 mW

Lead Temperature (T_L) (Soldering, 10 sec.)

240°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC}) 2.0V to 3.6V

Input Voltage (Vi)

0V to 5.5V

Output Voltage (VO)

OV to V_{CC} -40°C to +85°C

Operating Temperature (TA) Input Rise and Fall Time (Δ_t/Δ_v) 0 ns/V to 100 ns/V

General Description Vo S contains four 2-input AND gates. The inputs tot. Am 02 pt.t voltage level translation from 0.5 V 6 9 V 6.

Ordering Code: See Section 11

Package Number

DC Electrical Characteristics

	1110	7	157	4LVX0	8	741	LVX08		ļ je	
Symbol	Parameter	Vcc	TA	≠ +2	5°C		A = to +85°C	Units	Condi	tions
	0,8	7 4	Min	Тур	Max	Min	Max		A3	
V _{IH} 1-20211302-1	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4	TLIFA	V	B3	
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V		
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0	Description	1.9 2.9 2.48	Pin Nan	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36		0.1 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μА	$V_{IN} = 5.5V \text{ or GN}$	D
lcc	Quiescent Supply Current	3.6			2.0		20.0	μА	V _{IN} = V _{CC} or GNI)

legolici/KW

Noise Characteristics: See Sect	tion 2 for Test Methodology
---------------------------------	-----------------------------

			74L	80XV		
Symbol	Parameter	V _{CC}	T _A =	25°C	Units	C _L (pF)
		(*)	Тур	Limit	ARV	W IAS
VOLP	Quiet Output Maximum Dynamic V _{OL}	3.3	0.3	0.5	V	50
VOLV	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.3	-0.5	V	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	579.50	2.0	V	50
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	paign 19	0.8	V	50

trigger input. They are capable of transforming slowly at ideal for low power/low noise 3.3V appliance in the standard interfree output and score in the score in the standard interfree output and score in the score AC Electrical Characteristics: See Section 2 for Test Methodology

	mance	oheg blodse	74	LVXO	Bons prie	p-evillegg 74LV	X08	has hyst	The LVX14
Symbol	Parameter	V _{CC} (V)	T _A =	+ 25	th is de- tially 0°	-40°C to		Units	C _L (pF)
			Min	Тур	Max	Min olls V	Max	v ataralot	The inputs
t _{PLH} ,	Propagation Delay Time	2.7		6.3	11.4	1.0	13.5	ms to 3V	of Edhayste
t _{PHL}		2		8.8	14.9	1.0	17.0	no	50
		3.3 ±0.3		4.8	7.1	1.0	8.5	ons	15
	man	on Diag	doenne	7.3	10.6	1.0	12.0	seleny2	50
toslh, toshl	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. toSLH = |tpLHm - tpLHm|, toSHL = |tpHLm - tpHLn|

Capacitance

	9 511 4	-	74LVX0	В	74	LVX08	3	
Symbol	Parameter	Ty	A = +25	5°C	-40°C	20-4	Units	
	, e	Min	Тур	Max	Min	Max	7	in contract of
CIN	Input Capacitance	7	4	10		10		pF
C _{PD}	Power Dissipation Capacitance (Note 1)	- Carronal	18				1	pF

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{4 \text{ (per Gate)}}$

Truth Table

Output	Input				
	A				
Н					
	H				

SSOP TYPE I	SOIC EIAJ	SOIC JEDEC	
74LVX14MSCX	74LVX14SJ 74LVX14SJX	74LVX14M 74LVX14MX	
MSC14	MI4D	M14A	

74LVX14 Strat.s que

Low Voltage Hex Inverter with Schmitt Trigger Input

General Description

The LVX14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LVX14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications = d logal
- Available in SOIC JEDEC, SOIC EIAJ and SSOP
 packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Parameter

Symbol

pacitance,v.

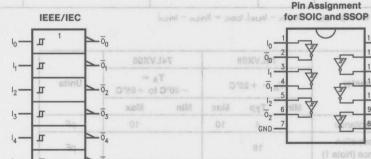
(1 alov) constitues TL/F/11603-1

Symbol

Ordering Code: See Section 11

Logic Symbol

Connection Diagram



TL/F/11603-2

Pin Names	Description
In	Inputs
\overline{O}_n	Outputs

Truth Table

Input	Output			
Α	ō			
L	Н			
Н	L			

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX14M	74LVX14SJ	
	74LVX14MX	74LVX14SJX	74LVX14MSCX
See NS Package Number	M14A	M14D	MSC14

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.						Recommended Operating Conditions Supply Voltage (V _{CC}) Input Voltage (V _I)			2.0V to 3.6V 0V to 5.5V		
	oltage (V _{CC})		gyT	-0.5V	Output Voltage	0V to 5.5V					
	C Input Diode Current (liv)							mperature (T _A) miss M is an 0 + 40°C to +85°C			
	1 = -0.5V						d Fall Time (Δ_t/Δ_v) 0 ns/V to 100 ns/V				
	ut Diode Curre	ent (IOK)		8.8			lynamic Input	Minimum High Level D	GHI		
	-0.5V V _{CC} + 0.5V	.0		3.3	-20 mA +20 mA		lynamic Input	Meximum Low Level D			
	ut Voltage (Vo			-0.5V to V _C				y = y = 3 as			
	out Source k Current (I _O)				±25 mA	S: See Section	steristic	ectrical Charac	AC Ele		
(I _{CC} or Storage Power D	or Ground Cur r I _{GND}) Temperature (issipation the "Absolute I	T _{STG})	= AT + of 3	-65°C to	+150°C 180 mW	$74LV$ $T_A = +$ $Min Typ$	(V)	Parameter	lodmyi		
beyond teed. Th paramet	which the safe e device should ric values defir	ety of the d not be ned in th	operatie "Elec	ce cannot be ted at these li ctrical Charac	guaran- imits. The cteristics"	8.7	2.7	Propagation Delay Time	PLH		
The "Re	e not guarante ecommended C ditions for actu	perating	g Condi	itions" table	will define	8.8 8.9	6,0± 8.8				
DC E	lectrical	Char	acte	ristics	1.5		2.7	Output to Output Skew (Note 1)	HISO HUSO		
			1-100 0000	74LVX14	laurer - muser	74LVX14	TOTAL = Itput	meter guaranteed by design.	Note 1: Pare		
Symbol	Parameter	Vcc	Т	A = +25°C	-4	T _A = 0°C to +85°C	Units	Conditions	Capac		
			Min	Тур М	ax Min	At MaxAT					
't+	Positive Threshold	3.0		0°88+ 01	2	0°39 2.2 A	V	Parameter	Symbol		
′t-	Negative Threshold	3.0	0.9	xeM	0.9	Typ Max	nint v	I anni Carracilarena			
/н	Hysteresis	3.0	0.3	1	2 0.3	1.2	V	CONTRACTOR OF THE PROPERTY OF	Mic		

Symbol	Parameter	meter V _{CC}	74LVX14 T _A = +25°C		74LVX14 T _A = -40°C to +85°C]qt = Hgr	Note it Parameter guaranteed by design. to		
							Units			
				Min	Тур	Max	Min	At MaxAT		
V _t +	Positive Threshold	3.0		= +85°C	2.2		⊃°32 2.2 _A T	V	Parameter	Symbol
V _t -	Negative Threshold	3.0	0.9	celvi	п	0.9		V	and Canadiana	
VH	Hysteresis	3.0	0.3		1.2	0.3	1.2	V	Journal Displace from	NIO I
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0	od from th	1.9 2.9 2.48	21 Jent capacitance v	V ternal equiva	VIN TO VIL OF VIH	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36	× Voc × fin ± 6 (per Gale)	0.1 0.1 0.44	V (respectively)	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μΑ	V _{IN} = 5.5V or GND	
Icc	Quiescent Supply Current	3.6			2.0		20	μА	$V_{IN} = V_{CC}$ or GNE)

Noise Characteristics: See Section 2 for Test Methodology	RITE	R	MILL				bsol	
---	------	---	------	--	--	--	------	--

	Conditions	re required, uctor Sales	s septys	74L	VX14	y/Aeros contact	is muital
Symbol	Parameter	officultions.	VCC	VITA =	25°C	Units	C _L (pF)
nnV of V	Output Voltage (Vo)	.5V to +7.0V)-(*/	Тур	Limit	oltage (Vo	Supply V
VOLP	Quiet Output Maximum Dynamic VOLT	Am 0s-	3.3	0.3	0.5	V ₂ O	50
VOLV	Quiet Output Minimum Dynamic VOL	-0.5V to 7V	3.3	-0.3	-0.5) egVloV	Juga 500
V _{IHD}	Minimum High Level Dynamic Input Voltage	A 00	3.3	(N	2.0	eby3 tu	50
VILD	Maximum Low Level Dynamic Input Voltage	Am 0S +	3.3		0.8	.0 V	50

Note: Input $t_r = t_f = 3 \text{ ns}$

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVX14	Am 02+	74LVX	14 Inemia		0 00 V 00
Symbol	Parameter	V _{CC} (V)	T _A = +25°C 001 + of 0		A 230			Units	C _L (pF)
			Min	Тур	Max	Rating niMere th	Max M	uloedh" e	Note: Th
t _{PLH} ,	Propagation	2.7		8.7	16.3	1.0	19.5	inich the i device sh	15
t _{PHL}	Delay Time	2.1		11.2	19.8	"ElectiOn! Char	23.0	c values d	50
		3.3 ±0.3		6.8	10.6	1.0	12.5	elbaeama	15
		3.3 ±0.3		9.3	14.1	1.0	16.0	tions for a	50
toslh,	Output to Output Skew (Note 1)	2.7			1.5	cteristics	11.50	ns	50

or Sink Current (Io)

Symbol Parameter

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

			74LVX1	4	niM	74LV	X14	nHit			
Symbol	Parameter	V T	A = +2	5°C		T _A			Units	Positive Threshold	+ ₁ V
		Min	Тур	Max	0.0	Min	Max	K an	0.8	Negative	-1V
CIN	Input Capacitance		4	10	-		10		pF	Threshold	
CPD	Power Dissipation	V	Set		8.0	1.2		2,3	0.6	Hysteresis	HV
AA 03- = H	Capacitance (Note 1)		21		0.1			9.1	pF	High Level	ноУ
But Off - In	AL .	3/			42752		01.34	102.153	11 10 10	THE THE PARTY I	

= AT

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{6}$ (per Gate) 0.0 0.8 by the equation of $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{6}$ (per Gate) 0.0 0.8 equation of $I_{CC(opr.)} = I_{CC(opr.)} = I_$



J.SV

Low Voltage Quad 2-Input OR Gate

General Description

The LVX32 contains four 2-input OR gates. The inputs toler- Input voltage level translation from 5V to 3V / = 0V ate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP pack-

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Diatributors for availability and apportioations.

■ Guaranteed simultaneous switching noise level and dynamic threshold performance

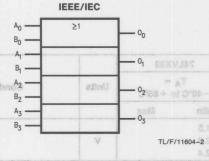
Ordering Code: See Section 11

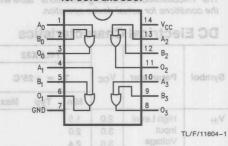
Logic Symbol

AH 01- = HO Au 08- = Hol Am 4- = HO! lot == 50 my lot = 50 MA tou as demy

Connection Diagram sted at those limits. The

Pin Assignment for SOIC and SSOP





A _n , B _n Inputs	Pin Names	Description
Outnute Outnute	A _n , B _n	Inputs
On Outputs	On	Outputs

8.0

INV AII	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX32M 74LVX32MX	74LVX32SJ 74LVX32SJX	74LVX32MSCX
NS Package Number	M14A	M14D	MSC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})

-0.5V to +7.0V

DC Input Diode Current (IIK) $V_1 = -0.5V$

-20 mA

DC Input Voltage (V_I)

-0.5V to 7V

DC Output Diode Current (IOK)

 $V_0 = -0.5V$

-20 mA

VO = VCC + 0.5Vnort notalenest level epatrov + 20 mA

DC Output Source I SOIC JEDEC, SOIC Elegrado Juquel Source

or Sink Current (IO)

±25 mA

DC V_{CC} or Ground Current (ICC or IGND)

Storage Temperature (TSTG)

-65°C to +150°C

Power Dissipation

180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not quaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define

Recommended Operating Conditions Semiconducti

Supply Voltage (V_{CC})

2.0V to 3.6V

Input Voltage (V_I)

0V to 5.5V

Output Voltage (Vo)

OV to Vcc

Operating Temperature (TA) Input Rise and Fall Time (Δ_t/Δ_v)

-40°C to +85°C 0 ns/V to 100 ns/V

General Description

Logic Symbol

The LVX32 contains four 2-input OR gates. The inputs toler-DC Output Voltage (Vo) each woll 19 + 0.5V to Vcc + 0.5V smellars Vd to example in gniwolfs VT of quiesgaflov eta

the conditions for actual device operation.

DC Electrical Characteristics

	28 -21 -			74LVX3	32	7	74LVX32		- Jan 18	
Symbol	Parameter	Vcc	TA	= +2	5°C	-40	T _A = °C to +85°C	Units	С	onditions
	1 9 Bs	0 1	Min	Тур	Max	Min	Max			
HIV	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4	UNO		1.5 2.0 2.4	TL/F/1180	V	(
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	v		
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0	Descripti inputs	1.9 2.9 2.48	Pin Names	v	V _{IN} = V _{IL} or	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \mu A$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0	1	0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	V _{IN} = V _{IL} or	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 \mu A$
IIN	Input Leakage Current	3.6			±0.1		±1.0	μΑ	V _{IN} = 5.5V o	r GND
Icc	Quiescent Supply Current	3.6	SSOP		0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5		74LVX32M	Aμ Number	V _{IN} = V _{CC} or	GND
			em .				M14A	okage	NS Pa	

Noise Characteristics: See Section 2 for Test Methodology

Noise	Characteristics: See Section 2 for Test Methodology		les	THAT S	Hold	PURE
			74LV	X32	Minnes	
Symbol	Parameter	V _{CC} (V)	T _A = :	25°C	Units	C _L (pF)
			Тур	Limit	XZA	ZALV
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.3	0.5	V.	50
VOLV	Quiet Output Minimum Dynamic VOL	3.3	-0.3	-0.5	V	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	Car a a -	2.0	V	50
VILD	Maximum Low Level Dynamic Input Voltage	3.3	noi	0.8	BOV IS	19/50

The LVX74 is a dual D-type flip-flop with Asynchronous is input voltage level translation from 5V

Clear and Set inputs and complementary (C, C) outputs. Wildest for low power/low noise 3.3V ap

Note: (Input $t_r = t_f = 3 \text{ ns}$)

AC Electrical Characteristics: See Section 2 for Test Methodology 1 of beneficial el Jugni edit la notamonal

Symbol	Parameter	V _{CC} one (V)	sed sirms reshold p	74LVX32 T _A = +25°C	is tocked of to the se input.	metensiii ed to	resent will n	ash egatio noitamo X Units il stuggi eur	ni bns tud CL (pF)
			Min	Тур	Max	MINHOLH	of CMaxe (te	ut to So (S	The second second
t _{PLH} ,	Propagation	2.7		5.8	10.7	1.0	12.5	Ut to Up (U	15
tPHL	Delay Time	2.1		8.3	14.2	drod 1.0 lem q	bn16.0 no	sons FOA	natiu508
		3.3 ±0.3		4.4	6.6	1.0	7.5	ns	15
		3.3 ±0.3		6.9	10.1	1.0	11.5	an Car	50
toshh	Output to Output Skew (Note 1)	2.7			1.5	TT HOUS	1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

	1 1 1 10	-	74LVX3	2	74	LVX32	
Symbol	Parameter	T,	A = +25	s°C		r _A =	Units
19 02	1 10 0 1 1 a a	Min	Тур	Max	Min	Max	
CIN O	Input Capacitance	5-4	4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 1)	UF/11606-4	14	mest av	17606-2	14/47	pF

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption

 $C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$ Average operating current can be obtained by the equation: I_{CC(opr.)} 4 (per Gate)

Package Number



74LVX74 Jimil

Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \(\overline{Q}\)) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

Maximum Low Level Dynamic Input Vol 2911

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages

Oulet Output Minimum Dynamic Vol.

Minimum High Level Dynamic Input Volt

Noise Characteristics: See Section 2 for Test Methodology

Guaranteed simultaneous switching noise level and dynamic threshold performance

LOW input to \overline{S}_D (Set) sets Q to HIGH level LOW input to \overline{C}_D (Clear) sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q}_D

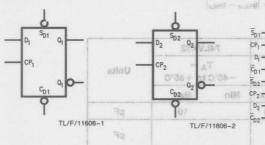
Ordering Code: See Section 11

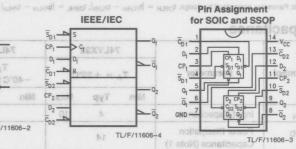
Logic Symbols

Connection Diagram

Symbol

DA





Truth Table (Each Half)

Pin Names	Description 201
D ₁ , D ₂	Data Inputs
CP ₁ , CP ₂	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
S _{D1} , S _{D2}	Direct Set Inputs
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs

	Inp	uts	banistric o	Out	puts
SD	¯c _D	СР	D	Q	Q
L	Н	Х	X	Н	L
Н	L	X	X	L	Н
L	L	X	X	Н	Н
Н	Н	_	Н	Н	L
Н	Н	_	L	L	Н
Н	Н	L	X	Q ₀	\overline{Q}_0

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

 $\mathcal{L} = \mathsf{LOW}\text{-to-HIGH Clock Transition}$ $\mathsf{Q}_0(\overline{\mathsf{Q}}_0) = \mathsf{Previous} \; \mathsf{Q}(\overline{\mathsf{Q}}) \; \mathsf{before} \; \mathsf{LOW}\text{-to-HIGH Transition of Clock}$

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX74M 74LVX74MX	74LVX74SJ 74LVX74SJX	74LVX74MSCX
See NS Package Number	M14A	M14D	MSC14

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage (Voc) -0.5V to +7.0V				emicond and spe	luctor S cification	Sales ns.	Supp		2.0V to 3.6V 0V to 5.5V				
	/oltage (V _{CC})	nLI e	Тур	-0).5V to +	7.0V	Input Voltage (V _I) 0V to 5. Output Voltage (V _O) 0V to V						
$V_1 = $	t Diode Curren	it (IIK)	0.3	8.8	-2	0 mA				re (T _A) mixsM fugtuO = 4	0°C to	0 +85°C/	
	t Voltage (V _I))— (8		3.3	-0.5V		Input	Rise and	Fall Tir	$me(\Delta_t/\Delta_v)$ 0 ns/	V to	100 ns/V	
The state of the s	out Diode Curre			8.8				Mi	ОНІУ				
	-0.5V	0		8.8		0 mA		-					
	V _{CC} + 0.5V 8 out Voltage (V _O				o V _{CC} +	0 mA		episiov in	dui ou	aximum Low Level Dynan	-	O'II_A	
DC Outp	out Source k Current (I _O)						Section	CSI See	iteh	trical Characte		AC EI	
	or Ground Cu r I _{GND})	rrent	74LVX			0 mA					-		
7567.556	Temperature (T _{STG})			°C to +1	50°C mW	Ŧ	(v)		Parameter		Symbol	
beyond teed. Th paramet	he "Absolute I which the safe ne device shoul tric values defir	ety of the Id not be ned in th	ne devi operati ne "Elec	ice cann ted at the ctrical Cl	ot be gu ese limits haracteris	aran- . The stics"	niM	2.7		opagetion Deley on to On or On		toHIT.	
The "Re	e not guarante ecommended C ditions for actu	perating	g Cond	litions" ta				3 ±0.3	3.				
DC E	lectrical	Char	acte	ristic	15.6	8.4		7.5		opagation Delay		H14)	
					1 0.01	0.01						71,7517	
-	an	0.0		74LVX7	4	7	4LVX7	4	-			3194	
Symbol	Parameter	12 23Vs	Т	74LVX7	1.01	8.0	4LVX7 T _A = C to +	8 ± 0.3	Unit	s Condition	ons	2000	
	Parameter		T	0.1	1.01	8.0	T _A =	8 ± 0.3	Unit	s Condition		W	
Symbol	Parameter	Vec	Min	0.1 A(F) +2	1.01 5°C _{0.81}	1 <u>2</u> 40°	T _A =	€.0± € 85°C	ε Unit		CF		
Symbol	Parameter High Level Input			0.1 A(F) +2	1.01 5°C _{0.81}	5.0 1.2.40°	T _A = C to +	85°C Max 7.5	^E Unit	on Con or Son	CF PE	W	
Symbol	Parameter High Level	Vec 2.0	Min 1.5	0.1 A → + 2 Typ	1.01 5°C _{0.81}	<u>40°</u> Min	T _A = C to +	85°C Max 7.2	8	n or Con or Son Ilse Width	CF PE	W	
Symbol /IH	Parameter High Level Input Voltage Low Level	2.0 3.0 3.6 2.0	Min 1.5 2.0	Typ 7 3.8	5°C _{3.81}	Min 1.5 2.0	T _A = C to + 3.8	8.0± 8 85°C Max ^{7.2} 8.0± 8 7.2 0.5	ε V	on or Con or Son tlee Widus stup Time	OF Pu Se	w	
Symbol /IH	Parameter High Level Input Voltage Low Level Input	2.0 3.0 3.6 2.0 3.0	Min 1.5 2.0	7 Typ 7 3.8 3.0	5°C 0.81 Max	Min 1.5 2.0	T _A = C to + 3.8 0 0.8 a.a. 3.0	8.0± 8 85°C Max ^{1,2} 8.0± 8 7.5 0.5 0.8	ε V	on or Con or Son tise Width stup Time to CP _n	Se Di Hu	w	
/ _{IH}	Parameter High Level Input Voltage Low Level Input Voltage	2.0 3.0 3.6 2.0 3.0 3.6	Min 1.5 2.0 2.4	**************************************	5°C _{3.81}	Min 1.5 2.0 2.4	T _A = C to + 2.8 8 8 0.8 2.8 2.0 2.0	85°C Max V.S 8.0± 6 7.S 0.5 V.S 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8	ε V	on or Con or Son tlee Width stup Time to CPn to CPn	Se D, Hc	W ³	
/ _{IH}	Parameter High Level Input Voltage Low Level Input Voltage High Level	2.0 3.0 3.6 2.0 3.6 2.0	Min 1.5 2.0 2.4	0.1 A(T) +2 OTyp V 6.8 8.0 8.0 8.0 8.2	5°C 0.81 Max	Min 1.5 2.0 2.4	T _A = C to + 3.8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	8.0± 8 85°C Max \S 8.0± 8 7.S 0.0± 8 0.5 0.8 0.8 0.8 0.8	E V	on or Con or Son thee Width Time To CFn to CFn to CFn to CPn To CPn To CPn To CPn To CPn	Se Da Ho	wi ≥i +ii = −50 μh	
/ _{IH}	Parameter High Level Input Voltage Low Level Input Voltage	2.0 3.0 3.6 2.0 3.6 2.0 3.6 2.0	Min 1.5 2.0 2.4 1.9 2.9	**************************************	5°C 0.81 Max	1.9 2.9	T _A = C to + 2.8 8 8 0.8 2.8 2.0 2.0	85°C Max V.S 8.0± 6 7.S 0.5 V.S 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8	E V	on or Con or Son thee Width Time To CPn co Son to CPn	Se Se De Ho	WI = -50 μA = -50 μA	
/IH /OH	High Level Input Voltage Low Level Input Voltage High Level Output Voltage	2.0 3.0 3.6 2.0 3.6 2.0 3.0 3.6	Min 1.5 2.0 2.4	**************************************	5°C 0.81 Max	Min 1.5 2.0 2.4	T _A = C to + 3.8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	8.0± 8 85°C Max S 8.0± 8 7.9 0.5 0.8 S 0.8 ± 8 6.0± 8	E V	stup Time to CP _n	Se Se H D H D H D H O F H O F H O F H O F O F O F O F O F	= -50 \(\mu \)	
/IH /IL	High Level Input Voltage Low Level Input Voltage High Level Output	2.0 3.0 3.6 2.0 3.6 2.0 3.0 3.0 3.0	Min 1.5 2.0 2.4 1.9 2.9	Typ 7 8.8 8.0 8.0 8.0 9.00 9.00 9.00	5°C 0.81 Max 0.5 0.8 0.8	1.9 2.9	T _A = C to + 3.8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	8.0± 8 85°C Max \S 8.0± 8 7.S 0.0± 8 0.5 0.8 0.8 0.8 0.8	E V	on or Con or Son the Widur of Con or Son the Widur of Con the Widur of Con the Widur of Con the Co	Se S	$= -50 \mu A$ $= -50 \mu A$ $= -4 \text{ mA}$ $= 50 \mu A$	
/IH /OH	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Low Level Output Voltage Low Level Low Level Low Level	2.0 3.0 3.6 2.0 3.6 2.0 3.0 3.6	Min 1.5 2.0 2.4 1.9 2.9	**************************************	5°C 0.81 Max	1.9 2.48	T _A = C to + 3.8 8 8 8 8.0 8.0 8.0 8.8 0.3 8.8	85°C Max \(^2\) 8.0 ± 8 7.8 0.5 0.8 7.8 0.80 ± 8 7.8 6.0 ± 8	8 V	on or Con or Son the Width attention atten	Se Se Se Se Se Se Se Se Se Se Se Se Se S	= -50 \(\mu \)	
/IH /OH	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Output Voltage	2.0 3.0 3.6 2.0 3.6 2.0 3.0 3.0 3.0 3.0 3.0	Min 1.5 2.0 2.4 1.9 2.9	Typ 6.8 8.0 8.0 8.0 8.0 8.0 8.0 8.0	5°C 0.81 Max 0.5 0.8 0.8	1.9 2.48	T _A = C to + 3.8	8.0 ± 8 85°C Max VS 8.0 ± 8 VS 0.8 VS 0.8 0 ± 8 0.1 VS 0.1	8 V	on or Con or Son the Width attention atten	Se Se Se Se Se Se Se Se Se Se Se Se Se S	$= -50 \mu A$ $= -50 \mu A$ $= -4 \text{mA}$ $= 50 \mu A$ $= 50 \mu A$	
Symbol VIH VIL	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Output Voltage	2.0 3.0 3.6 2.0 3.6 2.0 3.0 3.0 2.0 3.0 3.0	Min 1.5 2.0 2.4 1.9 2.9	7typ 6.8 8.0 8.0 8.0 8.0 8.0 8.0 8.0 8.0 8.0 8	0.5 0.8 0.8 0.8 0.1 0.1 0.36	1.9 2.48	T _A = C to + 2.8	85°C Max VS 8.0± 8 7.8 0.5 0.8 0.8 ± 8 0.1 VS 0.1 VS 0.1 0.44	E V S V	or Con or Son libe Widun the Con or Son	Hd Hd	$= -50 \mu A$ $= -50 \mu A$ $= -4 mA$ $= 50 \mu A$	

Noise Characteristics: See Section 2 for Test Methodology 2010 Septimes murmixable studeed A

	Conditions	ine required; luctor Sales	anopime	74L	VX74	contact	please
Symbol	Parameter		VCC	TA =	25°C	Units	C _L (pF)
apV of V	Output Voltage (Vo)	0.5V to +7.0V	-(-/	Тур	Limit	oltage (V	Supply V
V _{OLP}	Quiet Output Maximum Dynamic VoL	Am OS	3.3	0.3	0.5	V	50
Volv	Quiet Output Minimum Dynamic VOL	-0.5V to 7V	3.3	-0.3	-0.5	VolVige (ugn 50
V _{IHD}	Minimum High Level Dynamic Input Voltage	Am 00	3.3	(2)	2.0	ut Cyde	50
V _{ILD}	Maximum Low Level Dynamic Input Voltage	Am OS +	3.3		0.8	O +VOOV	50

Note: Input $t_r = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

					74LVX7	1 ₀₃₊		74LVX	74	UU D	or Groun	000 OCI
Symbol	Parameter		V _{CC} (V)				T _A = (araT) one -40°C to +85°C					C _L (pF)
				Min	Тур	Max	ans Ming	n Pati	Max	ute I		
t _{PLH} ,	Propagation Delay		2.7		7.3	15	1.0	RIGIDA NGO 81	18.5	nes hood	which the e device s	15
tPHL	CP_n to Q_n or \overline{Q}_n				9.8	18.5	0.110 0/10	els, el	22	defiir	estines	-m:50
			3.3 ±0.3		5.7	9.7	1.0	e sass a Cona	11.5	led C	nemman commen	15
					8.2	13.2	1.0	педо в	W45	เกิดเร	ilitions for	50
t _{PLH} ,	Propagation Delay		2.7		8.4	15.6	1.0	acte	18.5	le	lectric	15
tPHL	\overline{C}_{Dn} to \overline{S}_{Dn} to \overline{Q}_n or \overline{Q}_n	-		PARTER	10.9	19.1	1.0		22		ns	50
			3.3 ±0.3	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6.6	10.1	1.0		12		115	15
	Conditions	ežin	U DIE CO	+ 013	9.1	13.6	1.0	T	15.5	ref	Parane	50
t _W	CP_n or \overline{C}_{Dn} or \overline{S}_{Dn}		2.7 × 8.80	8.5	Min	xeM	10	aiM			ns	
	Pulse Width		3.3 ±0.3	6	1,5		7	1.6	0.5	lev	High Le	1-11
ts	Setup Time	V	2.7	8.0	2.0		9.5	2.0	3.0		fugni ns /	
	D _n to CP _n		3.3 ± 0.3	5.5	2.4		6.5	2,4	3.6		agsilay	
t _H	Hold Time	0	2.7	0.5		0.5	0.5		0.5	lei	ins i	ji
	D _n to CP _n		3.3 ± 0.3	0.5		8.0	0.5		3.6		Voltage	
trec	Recovery Time		2.7	6.5	1.9		0.7.5	0.1	2.0	lev	ns	но,
50 µA	CP _n or S _{Dn} to CP _n	¥	3.3 ± 0.3	5.0	2.9		5.0	2.9	0,8		Dunput	
f _{max}	Maximum Clock Frequence	су	2.7	55	135		50	8G.S	0.6		2511101	15
= 50 µA = 50 µA	TOI HIV OF NIV		1.0	45	60	0.1	40		0.5	191	MHz	50
Am 4 =			3.3 ±0.3	95	145	0.38	80		3.0		MHZ	15
	V _{IN} = 5.5V or GND	As	0.1±	60	85	1.0±	50		3.6		iuqni	50
toshh	Output to Output Skew (Note 1)		2.7			1.5			1.5	-	Leakag Can ent	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSLH} = |t_{PHLm} - t_{PHLn}|$

Capacitance

		74LVX74			74LVX74 T _A = -40°C to +85°C		ductor	A Semicon
Symbol	Parameter	T _A = +25°C		Units				
		Min	Тур	Max	Min	Max		74LVX86
CIN	Input Capacitance	DA	4	10	EXC	10 10	OS pF	Low Voltage
C _{PD}	Power Dissipation Capacitance (Note 1)		25	eatu			PFolia	General Descri

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption inputs tolerate voltages up to 7V all systems to 3V systems.

without load. Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2 \text{ (per F/F)}}$

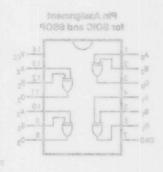
Guaranteed simultaneous switching noise level and dy-

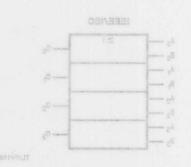
Ordering Code: See Section 11

BORNELL BORNE

Connection Diagram

Logic Symbol





Description	Pin Names
Inputs	eA-oA
	Bo-Bg
Outputs	pO-00

SSOP TYPE I	SOIC EIAJ	SOIC JEDEC	
74LVX86MSCX	74LVX86SJX 74LVX86SJX	74LVX86M 74LVX86MX	
MSC14	M14D	M14A	See NS Package Number



Low Voltage Quad 2-Input Exclusive-OR Gate

General Description

The LVX86 contains four 2-input exclusive-OR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

 $T_A = +26^{\circ}C$

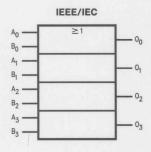
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

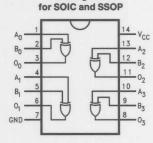
Logic Symbol

Connection Diagram

officetion blagram



TL/F/11605-2



Pin Assignment

TL/F/11605-1

Capacitance

Pin Names	Description				
A ₀ -A ₃	Inputs				
B ₀ -B ₃	Inputs				
00-03	Outputs				

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX86M 74LVX86MX	74LVX86SJ 74LVX86SJX	74LVX86MSCX
See NS Package Number	M14A	M14D	MSC14

2.0V to 3.6V

0V to 5.5V

OV to Vcc

Absolute Maximum Ratings (Note) Recommended Operating 40 ealow If Military/Aerospace specified devices are required, **Conditions** please contact the National Semiconductor Sales

Supply Voltage (V_{CC})

Output Voltage (Vo)

Operating Temperature (TA) 40°C to +85°C

Input Rise and Fall Time (Δ_t/Δ_v) 0 ns/V to 100 ns/V

Vec

Input Voltage (VI)

Office/Distributors for availability and specifications. Supply Voltage (VCC) -0.5V to +7.0VDC Input Diode Current (I_{IK}) $V_1 = -0.5V$ -20 mA DC Input Voltage (V_I) -0.5V to 7V

DC Output Diode Current (IOK) $V_0 = -0.5V$ -20 mA $V_{\rm O} = V_{\rm CC} + 0.5V$ +20 mA -0.5V to $V_{CC} + 0.5V$

DC Output Voltage (Vo) DC Output Source

AC Electrical Characteristics: See Section 2 to Am 25 ± ethodology or Sink Current (IO) DC V_{CC} or Ground Current (I_{CC} or I_{GND}) ±50 mA

-65°C to +150°C Storage Temperature (TSTG) **Power Dissipation** 180 mW 35 + = AT

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

				74LVX86		74LV	(86		ew (Note 1)			
Symbol	Parameter	Vcc	T	A = +25°C	T _A = decid = m -40°C to +85°C		Units	Conditions				
			Min	Тур Мах	Mir	1	Max		Capacitanes			
V _{IH}	High Level	2.0	1.5	PALVX86	1.5		74LVX86					
	Input Voltage	3.0	2.0	TA = °C to +65°C	2.0		T _A = +25	V	Parameter			
V _{IL}	Low Level	2.0	8= 1	xsM 0.5	rilli	хаМ	0.5	dilli -				
-	Input Voltage	3.0		0.8 0.8		10	0.8	V	Input Capacitance	OiN		
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 gridaringo erit most	1.9 2.9 2.48		18 lent capacitanos	vi.po iemo	V _{IN} = V _{IL} or V _{IH}	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 mA$		
V _{OL}	Low Level	2.0		0.0 0.1	eo × t _{in} +	Cen×V	0.1		V _{IN} = V _{IL} or V _{IH}	I _{OL} = 50 μA		
OL	Output Voltage	3.0		0.0 0.1 0.36	per (Sate)		0.1 0.1 0.44	V V	buildido ed Rao melles	$I_{OL} = 50 \mu A$ $I_{OL} = 4 \text{ mA}$		
I _{IN}	Input Leakage Current	3.6		±0.1			±1.0	μА	V _{IN} = 5.5V or GNI)		
Icc	Quiescent Supply Current	3.6		2.0			20.0	μΑ	V _{IN} = V _{CC} or GNE)		

Noise	Characterist	ics: See	Section 2 for	Test Me	thodolo	gyatol	ings	Rai	mumi	lute Maxi	Abso
		8	notition	CC		uper o		D 09	4LVX86	ry/Asrospace	stillM H
Symbol		Par	ameter	Sup		ctor S	ACC	VALLE	a = 25°0	Charles Units	C _L (pl
Va.a of VD		(ut Voltage (V	Inpi	7.0V	+ of Va	(V)	Ту		mito(V) epatio	Supply V
VOLP	Quiet Output Maxim	um Dynamic	Vol online	000	Am 0	10	3.3	0.3	3 0	.5 V	50
VOLV OOT			ynamic V _{OL}			Va.0-	3.3	-0	.3 –	0.5 V ep V oV	50
V _{IHD}	Minimum High Leve					3.3		(HOI) #2	ut Cyode Curo.	50	
VILD	Maximum Low Leve	I Dynamic In	put Voltage		Am 0	+21	3.3		0	.8 v V V	50
	t _r = t _f = 3 ns) ectrical Chara	acterist	ics: See S	Section 2			dology			ut Voltage (Vo) ut Source : Current (Io)	
345				74LVX	86 Am 0	是士	(6	74LVX	86		DO VOC
Symbol	Parameter	V _{CC} (V)	1	Γ _A = +:	25°C/m	-40°C		T _A =		Units	C _L (pl
			Min	Тур	-ne-N	lax	on Min	e devic	Max	which the safe	seyond
t _{PLH} ,	Propagation	2.7		7.5	1779	4.5	1.0	operat	17.5	r device should ic values d <mark>efin</mark>	15
tPHL	Delay Time	2.7		10.0	Ings.	8.0	1.0	oeda ed 21.0 a		not guarantes	50
		3.3 ± 0.3		5.8	enite	9.3	1.0	Condi	11.0	nsmorted of Children of the	15
		0.0 10.0		8.3	1	2.8	1.0		14.5		50
toshl	Output to Output Skew (Note 1)	2.7	88			1.5	PISTICS 74LVX86	SIOE	1.5	ns	50
	ameter guaranteed by designation	gn. tosch = tp		OSHL = t _t		PHLnl D	7 = +25	T	Yoc	Parameter	lodmy
			74LVX86	3		74LVX	36		0.9	High Level	
Symbol	Parameter	V	T _A = +25	r°C	S -40	T _A =		U ^{2,0}	nits	Input Voltage	
		M	п Тур	Max	Min	0.5	Max		2.0	Low Level	
CIN	Input Capacitano	ce	84	10		8.0	10		oF 0.8	Input Voltage	
C _{PD}	Power Dissipation Capacitance (No	Ast I	18		1	0.0	2.0	1.0	2.0 Po	High Level Output	HC
Note 1: C _{PD} without load.	is defined as the value of the	ne internal equiv	alent capacitano	e which is	calculated	d from the	operating c	urrent co	nsumption		
Average ope	rating current can be obtain	ned by the equ			oc × f _{IN} +	1.0	0.0		2.0	Low Level Output	
= 4 mA	and the second second second second		0,44			0.36			3.0		
	N = 5.5V or GND	V Au				1.0±			3.6	Input Leakage Current	



Low-Voltage Quad Buffer with TRI-STATE® Outputs DC Output Diede Current (lox)

General Description

The LVX125 contains four independent non-inverting buffers with TRI-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP

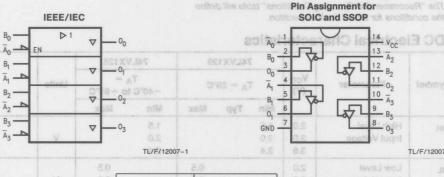
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

■ Guaranteed simultaneous switching noise level and dy-Organic threshold performance Trapped ama Tapanot?

Ordering Code: See Section 11

Logic Symbol

Connection Diagram



Description				
Inputs Outputs				

-=HOI HIV **Truth Table**

IOL = 4 II

Inputs		Output
An	Bn	On
L	Lone	L
L	H	Н
Н	X	Z

H = HIGH Voltage Level L = LOW Voltage Level

Z = High Impedance X = Immaterial

Ass

SOIC JEDEC SOIC EIAJ SSOP TYPE I Order Number 74LVX125M 74LVX125SJ 74LVX125MX 74LVX125SJX 74LVX125MSCX See NS Package Number M14A M14D MSC14

TL/F/12007-2

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) -0.5V to +7.0VDC Input Diode Current (I_{IK}) $V_{I} = -0.5V$ -20 mA

DC Input Voltage (V_I) -0.5V to +7.0V

DC Output Diode Current (IOK)

-20 mA +20 mA $V_0 = 0.5V$ $V_{\rm O} = V_{\rm CC} + 0.5V$

Output Voltage (VO) -0.5V to $V_{CC} + 0.5V$

DC Output Source/Sink Current (Io) ±25 mA

DC V_{CC} or Ground Current

(ICC or IGND) politorias suconstituras basins ±50 mA

Power Dissipation

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (VCC) Input Voltage (Vi)

2.0V to 3.6V 0V to 5.5V

Output Voltage (VO)

OV to Vcc

Operating Temperature (T_A) -40°C to $+85^{\circ}\text{C}$ Input Rise and Fall Time ($\Delta t/\Delta v$) 0 ns/V to 100 ns/V

Ordering Code: See Section 11

Logic Symbol

The LVX125 contains four independent non-inverting buff

DC Electrical Characteristics

	1 STE	7 4	_ oB 7	4LVX12	5	74LV	K125		B,	
	Parameter	V _{CC} (V)	$T_A = 25^{\circ}C$			T _A		Units	Conditions	
	e P	Y	Min	Тур	Max	Min	Max		Az-D	
V _{IH}	High Level Input Voltage	2.0 3.0	1.5			2.0	0	V	B ₃ — La A ₃ —	
L/F/12007-2		3.6	2.4		18	2.4				
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6	noll	Descript	0.5 0.8 0.8	Pin Names	0.5 0.8 0.8	V		
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	3.0		1.9 2.9 2.48		V	V _{IN} =V _{IL} or V _{IH}	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36	Inputs A ₀	0.1 0.1 0.44	V	V _{IN} =V _{IL} or V _{IH}	I _{OL} =50 μA I _{OL} =50 μA I _{OL} =4 mA
loz	TRI-STATE Output Off-State Current	3.6			±0.25	7	±2.5	μΑ	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	
I _{IN}	Input Leakage Current	3.6		Z	±0.1	H HIGH Vollage	±1.0	μА	V _{IN} = 5.5V or GND	
Icc	Quiescent Supply Current	3.6	4.0		= LOW Voltage = High Impedan = Immaterial	40.0	μА	V _{IH} = V _{CC} or GND		

SSOP TYPE I	SOIC EIAJ	SOIC JEDEC	
74LVX125MSCX	74LVX125SJ 74LVX125SJX	74LVX125M 74LVX125MX	Order Number
MSC14	M14D		See NS Package Number

V

			74LV	X125	Marchine		
Symbol	Parameter	V _{CC}	T _A = 25°C		Units	C _L (pF)	
		(*)	Тур	Limit	8017	W IN	
VOLP	Quiet Output Maximum Dynamic VOL	3.3	0.3	0.8	V	50	
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	-0.3	-0.8	REALCH	50	
VIHD	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50	

3.3

Note: Input $t_r = t_f = 3$ ns. Figure VE. 8 selon well reway well to

VILD

AC Electrical Characteristics: See Section 2 Test Methodology

Maximum Low Level Dynamic Input Voltage

	ACO	amoheq blo	daend 74L	.VX12	25	74	LVX125	nverter.	LVX138 devices and one	
Symbol	Parameter	V _{CC} (V)	T _A = +25°C				T _A = C to +85°C	Units	Conditions	
			Min '	Тур	Max	Min	Max			
t _{PLH} ,	Propagation Delay Time	2.7		5.8	10.1	1.0	13.5		C _L = 15 pF	
tPHL	Data to Output	2.7		8.3	13.6	1.0	17.0		$C_L = 50 pF$	
	Pin Assignment	3.3 ±0.3		4.4	6.2	1.0	8.5	ns	C _L = 15 pF	
	for SOIC and SSOP			6.9	9.7	31 1.0	12.0		C _L = 50 pF	
t _{PZH} ,	Output Enable Time	2.7	7	5.3	9.3	1.0	12.5		$C_L = 15 pF$, $R_L = 1 k\Omega$	
t _{PZL}	2 15 -00	- _I A	610	7.8	12.8	1.0	16.0		$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
	14 -0	3.3 ±0.3	- ō,	4.0	5.6	1.0	7.5	ns	$C_L = 15 pF$, $R_L = 1 k\Omega$	
	13 - 02	0.0 ±0.0	- 03	6.5	9.1	1.0	11.0	70 gO	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _{PHZ} ,	Output Disable	2.7	,0 -	10.0	15.7	1.0	19.0	991	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
tPLZ	Time	3.3 ± 0.3	20	8.3	11.2	1.0	13.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
toshl, toslh	Output to Output Skew (Note 1)	2.7	4 <u>0</u>	1	1.5	None of the last	1.5	ns	C _L = 50 pF	

Note 1: Parameter guaranteed by design. toSLH = |tpLHm - tpLHn|, toSHL = |tpHLm - tpHLn|

Capacitance

			74LVX125	74L	VX125		
Symbol	Parameter		T _A = 25°C	-40°C	Units		
		Min	Тур Мах	Min	Max		
CIN	Input Capacitance		4.0 ugal =10 m3		€ 10	pF	
C _{PD}	Power Dissipation Capacitance (Note 1)		14	1 70	-00	pF	

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{4 \cdot (c_{CD} + I_{|N})}$

	SOIG 1EDEC		SSOP TYPE I
Order Number		74LVX138SJ	
		74LVX138SJX	74LVX138MSCX
See NS Package Number	M16A	M16D	



Low Voltage 1-of-8 Decoder/Demultiplexer

General Description

The LVX138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVX138 devices or a 1-of-32 decoder using four LVX138 devices and one inverter.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages

Noise Characteristics: See Section 2 for Test Methodology

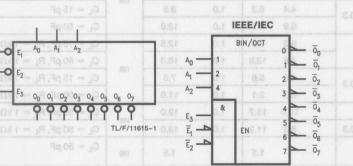
 Guaranteed simultaneous switching noise level and dynamic threshold performance

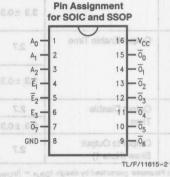
Ordering Code: See Section 11

Logic Symbols

Connection Diagram

Parameter





TL/F/11615-3

acitance

Symbol

Symbol

Pin Names	Description		
A ₀ -A ₂ E ₁ -E ₂	Address Inputs Enable Inputs		
E ₃	Enable Input		
$\overline{O}_0 - \overline{O}_7$	Outputs		

SOIC JEDEC SOIC EIAJ SSOP TYPE I

74LVX138M 74LVX138SJ

 Order Number
 74LVX138M 74LVX138MX
 74LVX138SJ 74LVX138MSCX
 74LVX138MSCX

 See NS Package Number
 M16A
 M16D
 MSC16

DC Output Source or Sink Current (Io)

beyond which the safety

Symbol Parameter Voc

Functional Description

The LVX138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs $(A_0,\,A_1,\,A_2)$ and, when enabled, provides eight mutually exclusive active-LOW outputs $(\overline{O}_0-\overline{O}_7)$. The LVX138 features three Enable inputs, two active-LOW $(E_1,\,E_2)$ and one active-HIGH (E_3) . All outputs will be HIGH unless \overline{E}_1 and \overline{E}_2 are LOW and E_3 is HIGH.

The LVX138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Absolute Maximum Ratings (Note)

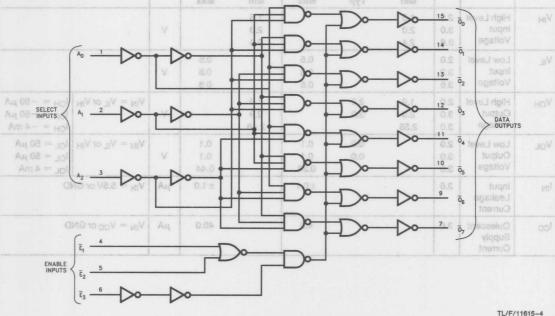
Truth Table

									A.m.	00			
		Inp	uts						Out	puts			
Ē ₁	E ₂	E ₃	A ₀	A ₁	A ₂	Ō ₀	Ō ₁	Ō ₂	O ₃	Ō ₄	Ō ₅	○ 0 6	Ō ₇
Н	X	X	X	X	X	Н	Н	Н	H	асН	Н	Н	Н
X	Н	X	X	X	X	Н	Н	Н	H	Н	Н	Н	Н.,
Χ	Х	L	X	Х	X	Н	Н	Н	H. 000	H	S. Har	H	HOU
L	L	н	L	L	L	L	н	н	HVIII	○SH	н	н	н
L	L	Н	Н	L	L	Н	L	Н	Hen	BY HE	all the	, stHyp	A spare
L	L	Н	L	Н	L	Н	Н	L	H	SUH S	10H	H	H
L	L	Н	Н	Н	L	Н	Н	Н	Ç _{ew.i}	H"H"S.	18/1/ /E	Howal.	do Hay
L	L	Н	L	L	н	н	н	н	H	itten mi	H	н	s off s
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	o Ha	H
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	aH	ei Hei	OCLE

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) DC Input Diode Current (I_{IK})

one med ed icom be -0.5V to +7.0V

 $V_I = -0.5V$

-20 mA

DC Input Voltage (VI)

-0.5V to 7V

DC Output Diode Current (IOK)

 $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ -20 mA +20 mA

DC Output Voltage (VO) DC Output Source or Sink Current (IO)

Power Dissipation

± 25 mA ±75 mA

DC V_{CC} or Ground Current (I_{CC} or I_{GND}) Storage Temperature (TSTG)

-65°C to +150°C

-0.5V to $V_{CC} + 0.5V$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

Conditions	noaeb 8-to-1 beega-rigin
manley have fall up a	Inary weighted inputs (A
Supply Voltage (V _{CC})	days allegiture triple pobl

2.0V to 3.6V Input Voltage (V_I) OV to 5.5V Output Voltage (Vo) who are the (et al.) WOJ OV to Vcc Operating Temperature (T_A) = 40°C to +85°C

Recommended Operating

			II Time)	0 ns/	V to 10	
					uts			
0.0	-,5		gA	1A		E3	Ez	
H	Н		X		X	X	X	
H				X				
н	H		X	×				
	н			1	J	Н		1
				1	-8	H	1	1
			1	H	1		1.2	J
		H		Н	H	Н		
			16		1			
H			H			Н	J	11
H			H	H		Н	1	1

				74LVX138		74LV	/X138			H = HIGH Voltage	
Symbol	Parameter	Vcc	1	T _A = +25°C			(= to +85°C	Units	Condi	tenstermi = X	
			Min	Тур	Max	Min	Max		Logic Diagram		
VIH	High Level	2.0	1.5	-0(T	790	1.5	9	V			
	Voltage	3.6	2.4	~~	1-0	2.4					
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6	~< ~ </td <td></td> <td>0.5 0.8 0.8</td> <td></td> <td>0.5 0.8 0.8</td> <td>V</td> <td></td> <td></td>		0.5 0.8 0.8		0.5 0.8 0.8	V			
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48	0	v	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$	
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0	~< ~<	0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$	
I _{IN}	Input Leakage Current	3.6	~	-CI	±0.1		±1.0	μА	V _{IN} = 5.5V or GN	ND	
Icc	Quiescent Supply Current	3.6	-4-	-<1	4.0		40.0	μА	V _{IN} = V _{CC} or GN	D	

эутроі	Parameter	(V)	T _A =	25°C	Units	(pF)	
		(*)	Тур	Limit	HWW	ZAI	
VOLP	Quiet Output Maximum Dynamic V _{OL}	3.3	0.3	0.5	V	50	
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	-0.3	-0.5	V	50	
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	meli	2.0	V	50	
VILD	Maximum Low Level Dynamic Input Voltage	3.3	D francis by	0.8	a e Vary	50	

AC Electrical Characteristics: See Section 2 for Test Methodology without such and at the habiteties and

	8	d performance	mio threshole	74LVX138		74L\	/X138		
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		-40°C 1	Units	C _L (pF)		
			Min	Тур	Max	Min	Max		
t _{PLH}	Propagation	2.7		7.1	13.8	1.0	16.5	smy2:	15
t _{PHL}	Delay Time A _n to O _n	2.1		9.6	17.3	1.0	20.0	ns	50
	A _n to O _n	3.3 ±0.3		5.5	8.8	1.0	10.5	115	15
	ov-lai	3.3 ±0.3		8.0	12.3	1.0	14.0		50
t _{PLH}	Propagation	2.7		8.8	16.0	1.0	18.5		15
t _{PHL}	Delay Time \overline{E}_1 or \overline{E}_2 to \overline{O}_n	8 - 21		11.3	19.5	1.0	22.0	1	50
	L1 01 L2 to On	3.3 ±0.3	97-	6.9	10.4	1.0	11.5	ns	15
		0.0 ± 0.0	Tananana	9.4	13.9	d£ 1.0	15.0		50
t _{PLH}	Propagation	2.7		8.7	16.3	1.0	19.5	Zo Zb	15
t _{PHL}	Delay Time E ₃ to O _n	8 - 040	PZminom	11.2	19.8	1.0	23.0	ns	50
5-80	L3 to On	3.3 ± 0.3		6.8	10.6	1.0	12.5	115	15
		0.0 ±0.3	Dymen-	9.3	14.1	1.0	16.0		50
toshl toslh	Output to Output Skew (Note 1)	2.7	L/F/11808-4	7	1.5		1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Canacitance

Capac	italice						
Symbol			74LVX138	SOUN Enert	74LV	X138	
	Parameter	T _A = +25°C			T _A	Units	
		Min	Тур	Max	Min	Max	
CIN	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 1)		LAT 34 02	03	SOIC VIE	1	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$



74LVX157 Low Voltage Quad 2-Input Multiplexer

General Description

The LVX157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVX157 can also be used as a function generator.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications

Moise Characteristics: See Section 2 for Test Methodology

Symbol

Capacitance

Symbol

- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Symbol Ordering Code: See Section 11 Logic Symbols **Connection Diagram Pin Assignment** for SOIC and SSOP IEEE/IEC 0.1 F. EN G1 015 -E 14 MUX loa 1a 10b 1b 10c 1c 10d 1d Ов Поь 116 116 Za.er Zd -I_{1d} 10 4 lod GND-RTL/F/11608-1 TL/F/11608-2 0. M1c TL/F/11608-4 Skew (Note 1)

	Pin Names	Description
	I _{0a} -I _{0d}	Source 0 Data Inputs
	Ina-Ind	Source 1 Data Inputs Enable Input
Lore X D	S = AT	Select Input
icro-	Za-Zd OWA-	Outputs
	neld oild	Min Typ Max

- PF	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX157M	74LVX157SJ	as the value of the internal
	74LVX157MX	74LVX157SJX	74LVX157MSCX
See NS Package Number	M16A	M16D	MSC16

Functional Description

The LVX157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (Ē) is active-LOW. When Ē is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVX157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the LVX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LVX157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table its A mumixs M stuload A

required, or Selec	Inputs						
.aEoliss	nio sa be	isb <mark>o</mark> lly a	sva 191 ava	office/I Z sirfbutc			
VO. H+ of	X	X	x (00	Supply Voltage (V			
L	Н	X	(All) [Usuni	O Input Diode C			
Am gs -	Н	X	Н	Va.0 _H = V			
AL of Agr	L	L	X	3C Input_Voltage			
L	L	H (%	OUR XILL (IC	Outspit Diode			

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

425 mA

tions.				stad at these limits. T somest Characteristic				
	loa	фА —		₽	rting Co device . Z	ipera Ictua	conditions for a	The "Re fine the
	l _{1a}	3 фВ	Z4FAX 182	74LVX157	1140	DITE	lectrical (200
	IlloneO lob	5 фА —		0°85 + = A1	Z _b		Parameter	
	Чь	11	200		1.5 2.0	2,0	High Level input Voltage	н∨
	loc	фА —		○	Z	2.0 3.0 3.6	Low Level Input Voltage	
$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \mu A$	PHY TO TIME THE PLOT	14 ^V	9.5	0.8		2.0 3.0 3.0	High Level. Output Voltage	
юц = 50 µA юц = 50 µA юц = 4 mA	$V_{IN} = V_{IL} \text{ or } V_{IH}$	13 6B —		DO 0 12	Zd		Low Level Output Voltage	
	ha V _{IM} = 5.5V or GNIC S	1^Do-	-	±.0.±				
	V _{IM} = V _{CC} or GNC	Aη	0.04	О — фА				
	Ē	15		фВ	TI	_/F/110	508-3	

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	×	-0.5V to +7.0V
DC Input Diode Current (I _{IK})	X	A I
$V_1 = -0.5V$	X	-20 mA
DC Input Voltage (V _I)		-0.5V to 7V
DC Output Diode Current (IOK)	H	

DC Output Source or Sink Current (I_O) ±25 mA

DC V $_{\rm CC}$ or Ground Current (I $_{\rm CC}$ or I $_{\rm GND}$) \pm 50 mA

Storage Temperature (T_{STG}) -65°C to +150°C Power Dissipation 180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.

Recommended Operating and formal Conditions revelopment and 25 to a 15 to XVV and T

Supply Voltage (V _{CC})	2.00 10 3.00
Input Voltage (V _I)	0\/ to 5 5\/
Output Voltage (Vo)	
Operating Temperature (T _A)	-40°C to +85°C
Input Rise and Fall Time (Δ_t/Δ_v)	0 ns/V to 100 ns/V

 $Z_a = E \circ (l_{1a} \circ S + l_{0a} \circ \overline{S})$

 $Z_b = E \circ (I_{1b} \circ S + I_{0b} \circ \overline{S})$

 $Z_c = \mathbb{E} \circ (I_{1c} \circ S + I_{0c} \circ \overline{S})$

 $Z_d = \mathbb{E} \circ (|t_d \circ S + |t_{0d} \circ S)$ A common use of the LVX157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The LVX157 can generate any four of the sateson different functions of two variables with one variables common. This is useful for implementing gating turnostic.

DC Electrical Characteristics

			74LVX157	74LV)	157		n!											
Symbol	Parameter	Vcc	T _A = +25°C	T _A = -40°C to +85°C												Units	Conditions	
			Min Typ Max	Min	Max													
V _{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4	1.5 2.0 2.4	-0(V	al ^l											
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6	0.5 8.0 8.0 8.0	1-0	0.5 0.8 0.8	V	o0 ¹											
VoH	High Level Output Voltage	2.0 3.0 3.0	1.9 2.0 2.9 3.0 2.58	1.9 2.9 2.48		V	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$										
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0	0.0 0.1 0.0 0.1 0.36	1-C	0.1 0.1 0.44	V 80 E1	$V_{IN} = V_{IL} \text{ or } V_{IH}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 \text{ mA}$										
IIN	Input Leakage Current	3.6	±0.1	0<	±1.0	μΑ	V _{IN} = 5.5V or GN	D										
lcc	Quiescent Supply Current	3.6	4.0	Section 2	40.0	μΑ	V _{IN} = V _{CC} or GNI)										

			74LV	X157	Semio	Maria .	
Symbol	Parameter	V _{CC}	T _A = 25°C		Units	C _L (pF)	
			Тур	Limit	THY	7ALV	
VOLP	Quiet Output Maximum Dynamic VOL	3.3	0.3	0.5	L V	50	
VOLV	Quiet Output Minimum Dynamic VOL	3.3	-0.3	-0.5	V	50	
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	6863	2.0	og V is	50	
VILD	Maximum Low Level Dynamic Input Voltage	3.3	ill C yed	0.8	ZA iV a bi	50 AT	

used primarily as a 6-bit edge-triggered storage register. It ideal for low power/low noise 3.37 applicate \$100 and \$100

AC Electrical Characteristics: See Section 2 for Test Methodology and least Action of the AC Electrical Characteristics and points of the AC Electrical Characteristics.

Symbol Parameter		d performance	nic threshol	74LVX157		74L\	/X157		
	Parameter	V _{CC} (V)	T _A = +25°C				to +85°C	Units	C _L (pF)
			Min	Тур	Max	Min	Max		
t _{PLH} , Propagation	2.7		6.6	12.5	1.0	15.5	symoo	15	
t _{PHL}	Delay Time	ni9		9.1	16.0	1.0	19.0		50
	In to Znas bna Off	3.3 ±0.3		5.1	7.9	1.0	9.5	ns	15
	18 Vot	1 0.3 10.3		7.6	11.4	1.0	13.0		50
t _{PLH} , Propagation	2.7		8.9	16.9	1.0	20.5		15	
tPHL	Delay Time S to Z _n	E	₃ 0	11.4	20.4	1.0	24.0	ns	50
	12-0-02	3.3 ±0.3	,0 ~~~	7.0	11.0	1.0	13.0		15
	20-911	3.3 ±0.3	22 married 22	9.5	14.5	1.0	16.5	111	50
t _{PLH} ,	Propagation	7 - 27	E) comes	9.1	17.6	1.0	20.5		15
tPHL	Delay Time E to Z _n	2.7	AD resistory	11.6	21.1	1.0	24.0	ns	50
TL/F/1107-2	3.3 ±0.3		7.2	11.5	1.0	13.5	115	15	
		0.0 ±0.0	8-100111GL	9.7	15.0	1.0	17.0		50
toshl,	Output to Output Skew (Note 1)	2.7			1.5	,a	1.5	ns	50

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$,

Capacitance

	5 xx by 15	74LVX157			35 5-74L	Units O	
Symbol	Parameter				-40°C		
	VV	Min	Тур	Max	Min	Max	
CIN	Input Capacitance		4	10	1	10	pF
CPD-T98111	Power Dissipation Capacitance (Note 1)		20				pF

Note 1: CpD is def	fined as the va	alue of the internal eq	uivalent capacitance w	hich is calculated from the operating	g current consumption
without load.	98097	SOIC EIAJ	SOIC JEDEC		
- International			A CONTRACTOR OF THE PARTY OF TH	the first property of the prop	

vera	age operating current can	be obtained by the e	quation: I _{CC(opr.)} = C	PD × VCC × fIN + ICC	
1	74LVX174MSCX				
	MSC16	MileD	MARK	sedmul/Lensylve Number	

Low Voltage Hex D Flip-Flop with Master Reset

General Description

The LVX174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP pack-

Noise Characteristics: See Section 2 for Test Motirodology

■ Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

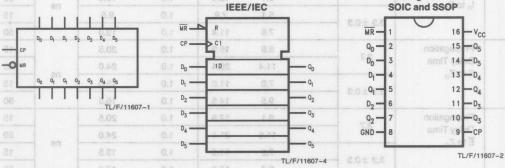
Logic Symbols

Connection Diagram

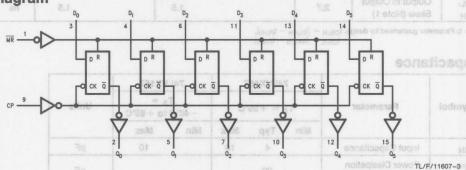
Pin Assignment for SOIC and SSOP

Symbol

Symidal



Logic Diagram



T	L	F	1	11	6	07	

Pin Names	Description
D ₀ -D ₅	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q ₀ -Q ₅	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX174M	74LVX174SJ	а орегалов сигета сво
	74LVX174MX	74LVX174SJX	74LVX174MSCX
See NS Package Number	M16A	M16D	MSC16

2.0V to 3.6V

0V to 5.5V

OV to VCC

Symbol

-40°C to +85°C

0 ns/V to 100 ns/V

Recommended Operating 10 acid

Output Voltage (Vo)

Conditions

Input Voltage (V_I)

Supply Voltage (Vcc)

Operating Temperature (T_A)

Input Rise and Fall Time (Δ_t/Δ_v)

AC Electrical Characteristics: See Section 2 for Test Methodology

Absolute Maximum Ratings (Note) polobodie M

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V	(cc)	Typ	0.5V to +7.0V
DC Input Diode C	current (I _{IK}	0.8 (
$V_1 = -0.5V$	-0.5	6.0-	-20 mA
DC Input Voltage	(V _I)		-0.5V to 7V
DC Output Diode	Current (ок)	

DC Output Source or Sink Current (I_O)

or Sink Current (I_O) ±25 mA

DC V_{CC} or Ground Current
(I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) -65°C to +150°C

Power Dissipation (P_D) 180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

				74LVX1	74	74L	VX174	8.0 ± 8.8	PO OF	
Symbol	Parameter	V _{CC}	Т,	A = +2	5°C		A = to +85°C	Units	Condition	ons H
			Min	Тур	Max	Min	Max	8.8 ± 0.8	ami'i levoore	
VIH	High Level	2.0	1.5	0,6		1.5	3.0	8.0 ± 6.8	R to GP	Ø
	Voltage -	3.0	2.0	7.6		2.0	8.8	V _S	lock Pulse ridth	
VIL	Low Level Input Voltage	2.0 3.0 3.6		7.5 5.0	0.5 0.8 0.8		0.5 0.8 0.8	2.7 3.8 ¥0.3	IR Pulse /idth	M W
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0		1.9 2.9 2.48	45 116	2.7 V 3.3 ±0.3	requency	$I_{OH} = -50 \mu$ $I_{OH} = -50 \mu$ $I_{OH} = -4 \text{mA}$
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36	36	0.1 0.1 0.44	٧	law (Note 1)	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$
I _{IN}	Input Leakage Current	3.6			±0.1	miller a	±1.0	μА	V _{IN} = 5.5V or GND	Capaciti
Icc	Quiescent Supply Current	3.6	#U	99.0	4.0		0.04 T _A = +26°C	μА	V _{IN} = V _{CC} or GND	Symbol
				X6		HER NUT	тур и	ruta		
									input Capacitance	

 $C_{PD} \times V_{CG} \times f_{IN} + f_{OC}$ 4 (per F/F)

Noise Characteristics: See Section 2 for Test Methodology and 32 miles of multiple of the Section 2 for Test Methodology

	Conditions	are required,	Vcc	74LV	/X174	POTORTY	and an
Symbol	Parameter Manual	**************************************		T _A = 25°C		Units	C _L (pF)
(V to 5.5V)	Input Voltage (V)),5V to +7.0V	(V)	Тур	Limit	V) epatio	Supply \
VOLP	Quiet Output Maximum Dynamic VOL		3.3	0.3	0.5	Didde C	50
V _{OLV}	Quiet Output Minimum Dynamic VOL	-20 mA	3.3	-0.3	-0.5	V	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	VV of Ve.0-	3.3		2.0	- Nov	50
V _{ILD}	Maximum Low Level Dynamic Input Voltage	Am ne	3.3	CHIC	0.8	V	50

Note: (Input $t_r = t_f = 3 \text{ ns}$)

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVX174	im as ±	74LVX	174	Current (lo	or Sink			
Symbol	Parameter	V _{CC} (V)	1	T _A = +25°	C 08 ±	T _A = -40°C to		Units	C _L (pF			
			Min	Тур	Max	Min	Max	l'emperatur	Storage			
t _{PLH}	Propagation	2.7		7.6	14.5	1.0	17.5	notisqies	15			
t _{PHL}	Delay Time CP to Qn	2.1		10.1	18.0	1.0	21.0	Absolu	50			
	Or to Qn	3.3 ± 0.3		5.9	9.3	1.0	11.0	en ns	15			
		3.3 ±0.3		8.4	12.8	Elec O.tal Cha	14.5	ic values di	50			
tpHL	Propagation Delay	2.7		7.9	15.0	1.0	18.5	stend tou	15			
	MR to Q _n	2.7		10.4	18.5	1.0	22.0	ns	50			
		3.3 ±0.3		6.2	9.7	1.0	11.5		15			
		3.3 IU.3		8.7	13.2	1.0	15.0	somoe	50			
ts	Setup Time	2.7	7.5	VIV. NAT	77	8.5						
	D _n to CP	3.3 ±0.3	5.0		200 mm in 1900 mm in 1	6.0	1	ns				
tH	Hold Time	2.7	0	AT TOWN	0	TA 0 +25	ooV 3		lodmy			
	D _n to CP	3.3 ±0.3	0			0	4					
t _{REM}	Removal Time	2.7	4.5	1616	XSSX	4.5						
	MR to CP	3.3 ±0.3	3.0	1.5		3.0	0.5	High Leve	141			
tw	Clock Pulse	2.7	6.5	2.0		7.5	3.0	ns _{ini} Voltage				
	Width	3.3 ±0.3	5.0	***		5.0	0.6	- obsauo v				
tw	MR Pulse	2.7	6.5		0.0	7.5	0.2	Low Level	.li			
	Width	3.3 ±0.3	5.0		0.0	5.0	0.6	ns				
f _{MAX}	Maximum	0.7	65	130	0.0	55	0.0		15			
	Clock To JV = M	2.7	45	60		40	0.8	High Leve	50			
$= -50 \mu A = -4 mA$	Frequency	00+00	115	180		95	0.0	MHz)	15			
	NO I	3.3 ±0.3	65	95	-	55			50			
toslh toshl	Output to Output Skew (Note 1)	2.7	1.0		1.5	0.0	1:5	ns	50			

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

	V _{BN} = V _{CC} or GND	74LVX174 T _A = +25°C			741	VX174	
Symbol	Parameter				T _A = -40°C to +85°C		Units
		Min	Тур	Max	Min	Max	
CIN	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 1)		29				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per F/F)}}$

3.6

74LVX240 Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVX240 is an octal inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP pack-

please contact the Mational Samioonductor Sales

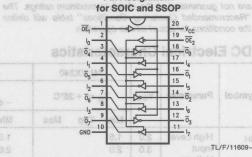
■ Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbol

Connection Diagram

Pin Assignment



TL/F/11609-1

IEEE/IEC	
OE, EN	
I ₀	_ ō₀ ō.
12	02 082XV.10
	03 = A7
OE ₂ — EN	Max
4 D V	\bar{o}_4 \bar{o}_5 \bar{o}_6
7	TL/F/11609-2

Pin Names Description OE1, OE2 TRI-STATE Output Enable Inputs 10-17 Inputs $\overline{O}_0 - \overline{O}_7$ Outputs

Truth Tables

Inpi	uts	-	Outputs		
OE ₁	In_	18 V	Outputs (Pins 12, 14, 16, 18)		
L	L	do.	A4 H		
L	H		L		
Н	X		Z		

-	Inpu	its	Outputs
	OE ₂	In	(Pins 3, 5, 7, 9)
	L	L	CHippit
	L	Н	OJI-State
	Н	X	Cgrent

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX240M 74LVX240MX	74LVX240SJ 74LVX240SJX	74LVX240MSCX
See NS Package Number	M20B	M20D	MSC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC)

-0.5V to +7.0V

DC Input Diode Current (IIK) $V_1 = -0.5V$

-20 mA

DC Input Voltage (V_I)

-0.5V to 7V

DC Output Diode Current (IOK) $V_0 = -0.5V$

-20 mA + 20 mA

 $V_O = V_{CC} + 0.5V$ DC Output Voltage (Vo)

-0.5V to $V_{CC} + 0.5V$

DC Output Source or Sink Current (IO)

± 25 mA

DC V_{CC} or Ground Current (ICC or IGND)

±75 mA

Storage Temperature (TSTG)

65°C to + 150°C

Power Dissipation (PD)

Note: Absolute Maximum Ratings are those values beyond which the safety to the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operarting Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

The LVX240 is an octal inverting buffer and line driver de-

driver and bus offented transmitter or receiver which pro-

signed to be employed as a memory address driver,

Supply Voltage (Vcc)

2.0V to 3.6V

Input Voltage (VI)

0V to 5.5V

Output Voltage (VO)

OV to Vcc

Operating Temperature (T_A) -40°C to +85°C Input Rise and Fall Time (Δt/ΔV)

0 ns/V to 100 ns/V

JIAIC.

General Description

DC Electrical Characteristics

	D 31	1-3	1/A	74LVX2	240	7	4LVX2	40	-4_	Control of the Contro	
Symbol	Parameter	Vcc	T,	= + 2	25°C	-40	T _A =	-85°C	Units	Conditi	ons
	12 05		Min	Тур	Max	Min		Max	l. L,	N3 - 30	
VIH	High Level	2.0	1.5	OHO .		1.5		a.C	- V	<	
1-60911750	Input	3.0	2.0			2.0			V	Same of	
	Voltage	3.6	2.4			2.4		9	- Anna -		
VIL	Low Level	2.0			0.5	n Kin	2-9081	0.5	-	No. of the Control of	
	Input	3.0			0.8			0.8	V		
	Voltage	3.6			0.8	w73		0.8	M sold	1	
VOH	High Level	2.0	1.9	2.0	utput Ens	1.9	1627)E ₂	2075	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu A$
	Output	3.0	2.9	3.0	aus indire	2.9			V		$I_{OH} = -50 \mu A$
	Voltage	3.0	2.58			2.48	aluO.		10-17 00		$I_{OH} = -4 \text{ mA}$
VoL	Low Level	2.0		0.0	0.1	CALLEST ACTIONS		0.1		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50 \mu A$
	Output	3.0		0.0	0.1			0.1	V	Tables	$I_{OL} = 50 \mu\text{A}$
	Voltage	3.0			0.36		of emily bender	0.44		and a committee	$I_{OL} = 4 \text{ mA}$
loz (8,	TRI-	3.6	al	1	±0.25			±2.5	t eniq)	$V_{IN} = V_{IH} \text{ or } V_{IL}$	30
	Output				1			EJ.	μА	$V_{OUT} = V_{CC}$ or GND	1
, 1 m 1	Off-State		H							H H	
	Current		X							X	H
I _{IN}	Input Leakage	3.6			±0.1	Z = Sligh	Ishatan	±1.0	μA	V _{IN} = 5.5V or GND	/ HOIH - H
	Current	BALL	000	1.0	13 O10 S	920	21-010	9			
Icc	Quiescent Supply	3.6	CA CAN		4.0	V 100 000 000	ALVX24		μΑιο	$V_{IN} = V_{CC}$ or GND	
	Current	240MS	VATA.			XIVIU				Control Control Control	

IonnHeMES

level egatioV HBIH - H

Noise Characteristics:	See Section 2 for Test Methodology
-------------------------------	------------------------------------

Symbol			74LV	X240	nimas	D. C.	
	Parameter	V _{CC}	T _A =	25°C	Units	C _L (pF)	
		(*)	Тур	Limit		74LV	
VOLP	Quiet Output Maximum Dynamic V _{OL}	3.3	0.5	0.8	V	50	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.5	-0.8	V	50	
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	2000	2.0	V	50	
VILD	Maximum Low Level Dynamic Input Voltage	3.3	no	0.8	V	50	

Note: (Input t_r = t_f = 3 ns) as a memory address driver, clock at Ideal for low power/low roise 3.3V approximants address driver, clock

AC Electrical Characteristics: See Section 2 for Test Methodology

	ing noise level and			4LVX24		74LV	X240	W system	7V allowing interisce of 5				
Symbol	Parameter	V _{CC} (V)	7	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions				
			Min	Тур	Max	Min	Max	See Sec	Ordering Code				
t _{PLH} ,	Propagation	u nono	Conne	5.7	10.1	1.0	12.5		C _L = 15 pF				
t _{PHL}	Delay Time		rij9	8.2	13.6	1.0	16.0	ns	$C_L = 50 pF$				
	90	3.3 ±0.3	5	4.3	6.2	1.0	7.5	ns	C _L = 15 pF				
	20 V - 02 1		- OE,	6.8	9.7	1.0	11.0		C _L = 50 pF				
t _{PZL} ,	TRI-STATE Output Enable Time		The state of the s			2.7	E 0	7.1	13.8	1.0	16.5	4	$C_L = 15 pF, R_L = 1 k\Omega$
t _{PZH}		Enable Time	Jan J	9.6	17.3	1.0	20.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$				
	5.31	3.3 ±0.3	B	5.5	8.8	1.0	10.5		$C_L = 15 \text{pF}, R_L = 1 \text{k}\Omega$				
	20 - 21 - 21	3.3 ±0.3	8 80	8.0	12.3	1.0	14.0		$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$				
t _{PLZ} ,	TRI-STATE Output	2.7	18	11.6	16.0	1.0	19.0	no	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$				
t _{PHZ}	Disable Time	3.3 ±0.3	CHO	9.7	11.4	1.0	13.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$				
toshh toshh	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C _L = 50 pF				

Note 1: Parameter guaranteed by design. toshh = |tphhm - tphhn|, toshh = |tphhm - tphhn|

Capacitance

		shuquis	74LVX24	10 10	741	30		
Symbol	rmbol Parameter		A = +2	5°C	T _A = -40°C to +85°C		- Units	
		Min	Тур	Max	Min	Max		
CIN	Input Capacitance	-	4	10		10	pF	
COUT	Output Capacitance	-1	6	1975		12, 14, 16, 16	pF	
C _{PD}	Power Dissipation Capacitance (Note 1)	3	17	10			pF	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{8 \text{ (per bit)}}$

SSOP TYPE I	SOIC EIAJ	SOIC JEDEC	
	74LVX244SJ 74LVX244SJX	74LVX244M 74LVX244MX	



Low Voltage Octal Buffer/Line Driver And Market Mar

(V)

General Description

The LVX244 is an octal non-inverting buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Noise Characteristics: See Section 2 for Test Methodology

Symbol

Syrni

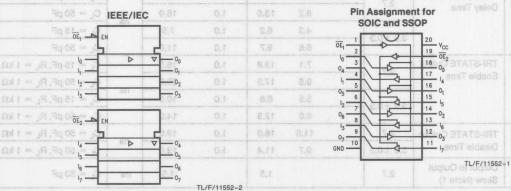
Capacitance

Symbol

Ordering Code: See Section 11

Logic Symbol

Connection Diagram



Pin Names

Description

OE₁, OE₂

Inputs
Inputs
O₀-O₇
Outputs

Truth Tables

Inpu	its	Outputs			
ŌĒ ₁	In	(Pins 12, 14, 16, 18)			
L	L	ild F			
L	н	Н			
Н	X no	ded from the oper Z ing ourrent consumbit			

-	Inp	uts	Outputs					
-	OE ₂	In 9	(Pins 3, 5, 7, 9)					
	01 L 71	L (I	Capacitance (Note					
alc	and doldw H nalloogs	tnelaviux lametr	Cop is defined Z the value of the					

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX244M 74LVX244MX	74LVX244SJ 74LVX244SJX	74LVX244MSCX
See NS Package Number	M20B	M20D	MSC20

please contact Office/Distribut Supply Voltage (N DC Input Diode (N I = -0.5V DC Input Voltage DC Output Source or Sink Current DC VCC or Groun (Icc or IgND) Storage Tempera Power Dissipation Note: The "Absorbeyond which the teed. The device parametric value table are not gua The "Recomment the conditions for DC Electri Symbol Param VIH High Le Input Voltage	tors for (V _{CC}) Current e (V _I) e Curren 0.5V age (V _O) ce tt (I _O) und Curr	r availab	MZAA	-0 8.8 8.8 8.8 -0.5V to	-20 -20 -20 -20 -20 -20 -20 -20 -20	mA 0.7V mA mA mA 0.5V	Supply Input \ Outpu Opera Input I	Rise and	e (V _{CC}) V _I) e (V _O) pperature (7 Fall Time (0	
DC Input Diode (V _I = -0.5V DC Input Voltage DC Output Diode V _O = -0.5V V _O = V _{CC} + (DC Output Voltage DC Output Voltage DC Output Voltage DC Output Source or Sink Current DC V _{CC} or Groun (I _{CC} or I _{GND}) Storage Tempera Power Dissipation Note: The "Absorbed Mich the tead. The device parametric value table are not guarthe "Recommer the conditions for DC Electri Symbol Param V _{IH} High Lo	Current e (V _I) e Curren 0.5V age (V _O) ce nt (I _O) und Curr	nt (lok)	0 	8.8 8.8 8.8 -0.5V to	-20 -0.5V to -20 +20 VCC + 0	mA mA mA mA 0.5V	Outpu Opera Input I	t Voltage ting Tem Rise and	perature (T	Γ _A) mixed fuction -40°C t Δt/ΔV) _{a just} 0 ns/V to	to +85°C
V _I = -0.5V DC Input Voltage DC Output Diode V _O = -0.5V V _O = V _{CC} + 0 DC Output Voltage DC Output Source or Sink Current DC V _{CC} or Groun (I _{CC} or I _{GND}) Storage Tempera Power Dissipation Note: The "Absorbeyond which the teed. The device parametric value table are not guarante the conditions for DC Electri Symbol Param V _{IH} High Le	e (V _I) e Currel 0.5V age (V _O) rce at (I _O) und Curr	nt (I _{OK})	-1 X244 -40°C	8.8 8.8 -0.5V to	-0.5V to -20 +20 0 V _{CC} + 0	mA mA .5V	Opera Input I	ting Tem	Fall Time (Γ _A) mixed fuction -40°C t Δt/ΔV) _{a just} 0 ns/V to	to +85°C
DC Input Voltage DC Output Diode Vo = -0.5V Vo = Vcc + C DC Output Voltage DC Output Source or Sink Current DC Vcc or Groun (Icc or IgND) Storage Tempers Power Dissipation Note: The "Absolute Able are not gue The "Recomment the conditions for DC Electri Symbol Param VIH High Le Input	e Currei 0.5V age (V _O) ace at (I _O) and Curr	nt (I _{OK})	X244 -40°C	6.8 -0.5V to	-0.5V to -20 +20 0 V _{CC} + 0	mA mA .5V	Input I	Rise and	Fall Time (Δt/ΔV) M jugtu 0 ns/V to	100 ns/V
DC Output Diode Vo = -0.5V Vo = Vcc + 0 DC Output Voltag DC Output Source or Sink Current DC Vcc or Groun (Icc or IgND) Storage Tempera Power Dissipation Note: The "Absorbeyond which the teed. The device parametric value table are not gua The "Recomment the conditions for DC Electri Symbol Param Vih High La Input	e Currei 0.5V age (V _O) ace at (I _O) and Curr	nt (I _{OK})	X244 -40°C	6.8 -0.5V to	-20 +20 o V _{CC} + 0	mA mA	9				
VO = VCC + O DC Output Voltag DC Output Source or Sink Current DC VCC or Groun (Icc or IgND) Storage Tempera Power Dissipation Note: The "Absolute table are not gua The "Recomment the conditions for DC Electri Symbol Param Vih High Le Input	ige (V _O) rce nt (I _O) und Curr	rent	X244 -40°C	-0.5V to	+20 0 V _{CC} + 0	mA 0.5V	9				
DC Output Voltag DC Output Source or Sink Current DC V _{CC} or Groun (I _{CC} or I _{GND}) Storage Tempera Power Dissipation Note: The "Absolute the device parametric value table are not gue The "Recomment the conditions for	ige (V _O) rce nt (I _O) und Curr	rent	X244 -40°C	-0.5V to	V _{CC} + 0).5V					
DC Output Source or Sink Current or Sink Curre	rce nt (I _O) und Curr	rent	X244 -40°C	ygok							
or Sink Current DC V _{CC} or Groun (I _{CC} or I _{GND}) Storage Tempera Power Dissipation Note: The "Absolute the Conditions for the Condition of the Condi	nt (I _O) und Curr		-40°C		obrit ±25	mAol S no				2 = 4 = 3 ns	Rote: Input
DC V _{CC} or Groun (I _{CC} or I _{GND}) Storage Tempera Power Dissipation Note: The "Absolute of the device parametric value table are not guate the conditions for the device parametric value table are not guate the conditions for the "Recommer the conditions for the "Becommer the "Becommer the conditions for the "Becommer the "Beco	and Curr		-40°C					es :80	teristic	ectrical Charac	AC EI
Storage Tempera Power Dissipation Note: The "Absoluted High Italian It	rature (T	STG)	-40°C	A.197							
Power Dissipation Note: The "Absolute Habe Devond which the teed. The device parametric value table are not guate the conditions for the condition	rature (T	STG)			±75	mA	ALVX2				
Note: The "Absubeyond which the beyond which the teed. The device parametric value table are not guar The "Recomment the conditions for DC Electri Symbol Parametric Parametric Parametric Parametric Voltage (Input Voltage)	2411750				°C to +15			a l	Vec	Parameter	lodmy
beyond which the teed. The device parametric value table are not gua the conditions for t				+ 01	180	mW			(V)		
teed. The device parametric value table are not gue the "Recommer the conditions for DC Electri Symbol Parametric Voltage input							Typ				
parametric value table are not gua The "Recommer the conditions for DC Electri Symbol Parametric Parametri Parametric Parametri Parametric Parametric Parametri Parametric Para							1.0		2.7	Propagation Delay	
The "Recommer the conditions for DC Electri Symbol Param Villa High Le Input Voltage							8.6			Time	
DC Electri Symbol Param High Le							4.7		8.0 ± 8.8		
DC Electri Symbol Param All High Lo					ible Will de	etine	7.2				
Symbol Param			-								
Param	ical (Chara	cter	istic	S		7.1		2.7	TRI-STATE Output	'7Ze
Param /IH High Le			7	74LVX2	244	7	4LVX24	14		Sint Globita	142
And t = 10 And t = 14 And t = 15 And t	Symbol Parameter V _{CC}		2		0.1	17.3	T _A =				
V _{IH} OS = High Le			T _A = +25°C			-40°C to +85°C		Units	Conditions		
Input Voltage		8.0	Min	Тур	Max	Min	6.0	Max	0.0 2 0.0		
Input Voltage	ovol	2.0	1.5			8.91.5	0.8				
Voltage	CVCI	3.0	2.0		1.0	2.0			V		
		3.6	2.4		0.1	2.4	11.6		2.7	TRI-STATE Output	.T.10
Low Le		2.0	7		0.10.5	11.4	9.7	0.5	8.0 ± 8.8	Disable Time	ZHe
Input Voltage	je	2.0			0.8	1.6		0.8	V		HJBC
OH High Le	ge	3.0	1.9	2.0	lenual	1.9	naet la		H-02 VHJ80	114 114 114 011	= -50 j = -50j

0.1

0.44

±2.5

±1.0

40.0

Mall

٧

μΑ

μΑ

μΑ

0.1

 $V_{IN} = V_{IH} \text{ or } V_{IL}$

 $V_{IN} = V_{IH} \, \text{or} \, V_{IL}$

 $V_{OUT} = V_{CC}$ or GND

Input Capacitance

 $V_{\text{IN}} = 5.5 \text{V or GND}$

 $V_{IN} = V_{CC}$ or GND

 $I_{OL} = 50 \, \mu A$

 $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$

VOL

loz

IIN

Icc

Low Level

TRI-STATE

Output Off-State

Current

Leakage

Current Quiescent

Supply Current

Input

Output Voltage 2.0

3.0

3.0

3.6

3.6

PF

3.6

0.0

0.0 0.1

0.1

0.36

 ± 0.1

4.0

±0.25

Noise Characteristics: See Section 2 for Test Methodology 1001 and 1012 and

	Conditions	ere required, fuctor Sales	essiven	74L\	/X244	ry/Aeros contact	esselu
Symbol	Parameter	cifications	Voc	T _A = 25°C		Units	C _L (pF)
noV of VC	(_A V) spailoV rugluO	0.5V to +7.0V	- (-/	Тур	Limit	(V) egatio	Supply \
V _{OLP} +	Quiet Output Maximum Dynamic VOL	Am OS-	3.3	0.5	0.8	V	50
VOLV OO	Quiet Output Minimum Dynamic VOL	V7 of V8.0 -	3.3	-0.5	-0.8	- VoVage	ugn 50]
V _{IHD}	Minimum High Level Dynamic Input Voltage	No. 00	3.3	(MC	2.0	eboy iu	50
V _{ILD}	Maximum Low Level Dynamic Input Voltage	Am OS +	3.3		0.8	0 - V - V	50

Note: Input $t_r = t_f = 3 \text{ ns}$

AC Electrical Characteristics: See Section 2 for Test Methdology

			7	4LVX2	44 Am	74L\	/X244	round Gu	DC V _{CC} or G
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		er + of OTA =	-40°C (STST	D 650	Conditions	
			Min	Тур	Max	lav eeMinesa ":	Max wind	Absolute I	Note: The "
t _{PLH} ,	Propagation Delay	2.7		6.1	11.4	1.0	13.5	h the sat doe show	$C_L = 15 pF$
t _{PHL}	Time			8.6	14.9	cal Of 0.1 cterist	ndoeld 17.0 ni beat	slues defin	$C_L = 50 pF$
		3.3 ± 0.3		4.7	7.1	1.0	8.5	sinens D'bebner	$C_L = 15 pF$
				7.2	10.6	1.0	12.0 00 18	s for actu	C _L = 50 pF
t _{PZL} , t _{PZH}	TRI-STATE Output Enable Time	2.7		7.1	13.8	1.00158	16.5	Isoin	$C_L = 15 \text{ pF}$ $R_L = 1 \text{ k}\Omega$
	Conditions		24	N.VX2		PESSAN			$C_1 = 50 pF$
		ofield		9.6	17.3	1.0	20.0	ns	$R_L = 1 k\Omega$
		3.3 ±0.3	Mant -	5.5	8.8	Typ 0.1	10.5	to IIS	$C_L = 15 pF$ $R_L = 1 k\Omega$
		v		8.0	12.3	1.0	0.5 14.0 S	level n	$C_L = 50 \text{ pF}$ $R_L = 1 \text{ k}\Omega$
t _{PLZ} ,	TRI-STATE Output	2.7		11.6	16.0	1.0	19.0	egal	$C_L = 50 pF$
t _{PHZ}	Disable Time	3.3 ± 0.3	0.6	9.7	11.4	8.01.0	13.0	ns level v	$R_L = 1 k\Omega$
toshh,	Output to Output Skew (Note 1)	2.7	8.0		1.5	8.0	1.5 0.8	ns	C _L = 50 pF

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

		74LVX244 T _A = +25°C			74LV	X244	9.8
Symbol	Parameter IV 30 Ja V = Ja V				-40°C t	Units	
	Vour = Voc or GND	Min	Тур	Max	Min	Max	
CIN	Input Capacitance		4	10		10	pF
COUT	Output Capacitance	Au	6		1.0±	***************************************	pF
C _{PD}	Power Dissipation Capacitance (Note 1)		19				pF

Note 1: Cpp is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{8 \text{ (per bit)}}$

V\sn

A4 08 - = HO! 10H = - 80 MA

iot = 80 µA

lot = 20 my IoL = 4 mA

Low Voltage Octal Bidirectional Transceiver

General Description

The LVX245 contains eight non-inverting bidirectional buffers is intended for bus-oriented applications. The Transmit/ Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH-Z condition.

Features

- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages Va.
- Guaranteed simultaneous switching noise level and Am dynamic threshold performance (a) memuo sinila to

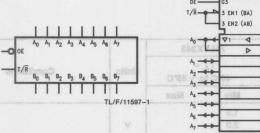
Note: The "Absolute Meximum Retings" are those values

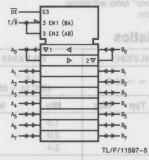
Ordering Code: See Section 11

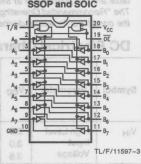
Logic Symbols

Connection Diagram

Pin Assignment for SSOP and SOIC







	Pin Names	8.0 Description	0.8
V	ŌĒ T/R	Output Enable Input Transmit/Receive Input	0.9
	A ₀ -A ₇ B ₀ -B ₇	Side A TRI-STATE® Inputs or TRI-STATE Output Side B TRI-STATE Inputs or TRI-STATE Outputs	

Truth Table

	Inpu	ts	Outputs
5.	ŌĒ	T/R	as.0.2Outputs
	L	L	Bus B Data to Bus A
	L	Н	Bus A Data to Bus B
	H OFF	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

V 0.05	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX245M 74LVX245MX	74LVX245SJ 74LVX245SJX	74LVX245MSCX
See NS Package Number	M20B	M20D	MSC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})

-0.5V to +7.0V

DC Input Diode Current (IIK)

 $V_1 = -0.5V$

-20 mA

DC Input Voltage T/R, OE (VI)

-0.5V to 7V

DC Diode Current (IOK)

 $V_{O} = -0.5V_{OB} \ VEE as$ $V_{O} = V_{CC} + 0.5V$

woo wol to la-20 mA

DC Bus I/O Voltage (VI/O) DC Output Source

-0.5V to $V_{CC} + 0.5$ V # Gueranteed simultane

or Sink Current (IO)

DC V_{CC} or Ground Current (ICC or IGND)

 $\pm 75 \, \text{mA}$

Storage Temperature (TSTG)

-65°C to +150°C

Power Dissipation

180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (Vcc)

2.0V to 3.6V 0V to 5.5V

Input Voltage T/R, OE (VI) Bus I/O Voltage (VI/O)

OV to Vcc

Operating Temperature (T_A) Input Rise and Fall Time (Δt/ΔV)

40°C to +85°C 0 ns/V to 100 ns/V

The LVX245 contains eight non-inventing bidirectional buil-

HIGH) enables data from A ports to B ports, Receive (ac-

Ordering Code: See Section 11

DC Electrical Characteristics

6.0		En.		74LVX245	74	LVX245	1	the sty the sty sty by the	20 0-	
Symbol	Parameter	Vcc	T,	A = +25°C	100	T _A = C to +85°C	Units	Cond	itions	
24		Ng seed	Min	Тур Мах	Min	Max	A TORRAGO			
V _{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4	1/8/11897-8 4-4-9-9	Market Commission of the Commi	4-3 M	V			
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6		0.5 0.8 0.8	160	0.5 0.8 0.8	nlý semsii			
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 aug	2.9	Cuipur Ens Trapsmit/R Side A TRI Side B TRI	7/5 A ₀ V _{A7} Ba-B7	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$	
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.1 0.0 0.1 0.36		0.1 0.1 0.44	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 \text{ mA}$	
loz	TRI-STATE Output Off-State Current	3.6		Bus A Date to B	R		μА	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } G$	iND	
I _{IN}	Input Leakage Current	3.6	lanata	elast Z ±0.1	K LOW Voll	±1.0	μА	V _{IN} = 5.5V or GND		
Icc	Quiescent Supply Current	3.6	950 74LV	74LVX245SJ 74LVX245SJ	C JEDEC VX245M VX245MX	40.0	μА	V _{IN} = V _{CC} or GN	D	
		15020	A	CIOSM	MIZOB	Number	S Package	See NS		

The section 2 to the section 2 to test well outload	Noise	Characteristics:	See Section 2 for Test Methodology
---	-------	-------------------------	------------------------------------

			74LVX245		noolm		
Symbol	Parameter	V _{CC} (V) T _A = 25°C			Units	Conditions C _L (pF)	
		(-)	Тур	Limit	573	XATAZ	
VOLP	Quiet Output Maximum Dynamic V _{OL}	3.3	0.5	0.8	V	50	
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	-0.5	-0.8	V	50	
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	wi-Cl bow	2.0	V	50	
VILD	Maximum Low Level Dynamic Input Voltage	3.3		0.8	brayand	1 0 1 50 VI	

The register is fully edge-triggered. The state of each D in-

Note: Input $t_r = t_f = 3 \text{ ns}$

AC Electrical Characteristics: See Section 2 for Test Methodology

			74LV	X245	74LVX	245	i WOJI i	put All outputs will be forced	
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A =	+85°C	Units	Conditions State	
			Min Ty	р Мах	Min	Max	stesM b	required and the Clock an	
t _{PLH}	Propagation Delay Time	2.7	6.	1 10.7	1.0	13.5	BV syste	C _L = 15 pF a to contact	
tPHL		2.7	8.	6 14.2	1.0	17.0		C _L = 50 pF	
		3.3 ±0.3	4.	7 6.8	1.0	8.0	ns se see	C _L = 15 pF	
	emperation (Nonday)	0.0 ± 0.0	7.	2 10.1	1.0	11.5		C _L = 50 pF	
t _{PZL}	TRI-STATE Output	2.7	9.	16.9	1.0	20.5		$C_L = 15 pF, R_L = 1 k\Omega$	
t _{PZH}	Enable Time		11	5 20.4	1.0	24.0		$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
		Pin Apsignment for SOIC and SSOP	3.3±0.3	7.	1 11.0	1.0	13.0	ns	$C_L = 15 pF, R_L = 1 k\Omega$
	pro-formania -	3.3±0.3	9.	6 14.5	1.0	16.5	1.1	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _{PLZ}	TRI-STATE Output	2.7	11	5 18.0	1.0	21.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
t _{PHZ}	Disable Time	3.3 ±0.3	9.	6 12.8	1.0	14.5	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$	
toslh toshl	Output to Output Skew (Note 1)	2.7	10 mmm	1.5	0,000	1.5	ns	C _L = 50 pF (Note 1)	

Note 1: Parameter guaranteed by design, toSLH = |tpLHm - tpLHn|, toSHL = |tpHLm - tpHLn|

Capacitance

albara.					
Symbol	40 -11 01 - 040	74LVX245	74LVX245	Units	
	Parameter	T _A = +25°C	T _A = -40°C to +85°C		
		Min Typ Max	Min Max		
CIN	Input Capacitance T/R, OE	neligi 4200 10	80 10 H 15	pF	
C1/0	Output Capacitance An, Bn	Data Inguts	γG- ₀ G	pF	
C _{PD}	Power Dissipation Capacitance (Note 1)	Clock 1215s Input:	90 90	pF	

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N|} + I_{CC}}{g_{COPR.}}$ opr.) = 8 (per bit)

Low Voltage Octal D Flip-Flop

Voc

General Description

The LVX273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

TL/F/11614-1

Features

TA = + 25°C

■ Input voltage translation from 5V to 3V

Parameter

- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages

Noise Characteristics: See Section 2 for Test Methodology

Symbol

Symbol

Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Q1 Q2 Q3 Q4

Logic Symbols

Connection Diagram

IEEE/IEC

Q

Q7

TL/F/11614-4

MR R
CP C1

D0 1D Q0

D1 Q1

D2 Q2

D3 Q3

D4 Q4

D5 Q5

20 - Vcc 19 - 07 18 - D7 Do 17 -Dg O D 16 - Q6 Q 15 -Q5 Q2 D_2 14 - D₅ D3 -913 -D4 08010 Q3 12 - Q4 GND 10 11 - CP

TL/F/11614-2

Pin Assignment for SOIC and SSOP

	Pin Names	Description			
19	Fill Names	Description			
la .	D ₀ -D ₇	Data Inputs			
	MR	Master Reset			
9	CP	Clock Pulse Input			
-	Q ₀ -Q ₇	Data Outputs			

D₆

D7 .

 SOIC JEDEC
 SOIC EIAJ
 SSOP TYPE I

 Order Number
 74LVX273M 74LVX273MX
 74LVX273SJ 74LVX273SJX
 74LVX273MSCX

 See NS Package Number
 M20B
 M20D
 MSC20

	ľ	1	9	1	

Res	set (Clear	JOHNOOLS SHE PL	serines se	X	X	A0.7+	Lat V3.	0-	H = HI	GH Voltage Level	Supply V
Loa		Hating Conditions	aded Ope	50008	" enH	Am DC	Н		X = Im	W Voltage Level	
Loa	ad '0'	Levice operation.	jenjoe 10	-	oo ent	VT of 1	La.o-		<i>_</i> =	material LOW-to-HIGH Transition	
Logic Va.s or V	c Diag	gram		dition Voltage	Cor	Am os Am os Ve.0		D ₅		Ut Diade Curent (lox) V8.0 - V8.0 + OOV Ut V6.0 + OOV Ut V6.0 + OOV D6 (V0)	
00 V CP'- 0°28 + 6 V\an 00	->0-	140 011	D Q CP RD	D CP RD		Q R _D	D Q	atte	O Q CP	(Current (IQ)	DC Vcc
	Please note	40	provided only	wold	Y 02	world		Q ₄	be used to		Q ₇ /F/11614-3
			V		1.5 2.0 2.4			1.5 2.0 2.4	2.0 3.0 3.6	High Level Input Voltage	H
		V _{IN} = V _{IH} or V _{II}							2.0 3.0 3.0	High Level Output Voltage	
	lot =		V	0.1 0.1 0.44		0.1 0.1 0.36			2.0 3.0 3.0	Low Level Output Voltage	
V _{IN} = 5.5V or GND		Aaş			±0.1						
	GN	V _{IN} = V _{CC} or G									
								See See	ics:	o Characterist	Noise
		78LVX273									
		TA = 25°C									
		Typ Limit									
	V									Quiet Output Maximi	
				Quiet Output Minimum Dynamic Vot							
08										Quiet Output Minimu	VJO/
-										Quiet Output Minimu Minimum High Level	OFFA

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) | epaticy HOIH = H -0.5V to +7.0V DC Input Diode Current (IjK) $V_1 = -0.5V$ -20 mA DC Input Voltage (V_I) -0.5V to 7V

DC Output Diode Current (IOK) $V_0 = -0.5V$ -20 mA $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (VO) -0.5V to $V_{CC} + 0.5V$ DC Output Source or Sink Current (IO) ±25 mA

DC V_{CC} or Ground Current (ICC or IGND) Storage Temperature (TSTG) **Power Dissipation**

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Mode Select-Function Table

2.0V to 3.6V

0V to 5.5V

Recommended Operating Conditions

Supply Voltage (V_{CC}) Input Voltage (V_I) Output Voltage (Vo)

OV to Vcc Operating Temperature (TA) -40°C to +85°C Input Rise and Fall Time (\Delta t/\Delta V) 0 ns/V to 100 ns/V

DC Electrical Characteristics

2	9 4	2	49	74LVX2	273	74LV	X273	7	4		
Symbol	Parameter	Vcc	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions		
F/11614-3	UT susiah nalisananna stambleb n	t kopu oz	Min	Тур	Max	Min	Max	no hohiso	a ai mannalh aidi ted atoota	Planaea	
V _{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V			
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V			
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		٧	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 mA$	
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$	
loz	TRI-STATE® Output Off-State Current	3.6			±0.25		±2.5	μΑ	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μΑ	V _{IN} = 5.5V or GND		
Icc	Quiescent Supply Current	3.6			4.0		40.0	μА	$V_{IN} = V_{CC}$ or GN	D	

±75 mA

180 mW

-65°C to +150°C

Noise Characteristics: See Section 2 for Test Methodology

Symbol			74LVX273 T _A = 25°C		Units	C _L (pF)
	Parameter	V _{CC}				
		(*)	Тур	Limit		
V _{OLP}	Quiet Output Maximum Dynamic VOL	3.3	0.5	0.8	V	50
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	-0.5	-0.8	V	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
VILD	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: Input $t_r = t_f = 3 \text{ ns}$

						74	LVX273	Units	C _L (pF)		
Symbol	Parameter	V _{CC} (V)					T _A = C to +85°C				
			Min	Тур	Max	Min	Max	K373	V sel 4		
t _{PLH}	Propagation	2.7	aten	9.0	16.9	1.0	20.5	STION	15		
tPHL	Delay Time CP to Q _n	2.1		11.5	20.4	1.0	24.0	ns	50		
	OF to Qn	3.3 ±0.3		7.1	11.0	1.0	13.0		15		
	Name of the last	3.3 IU.3	29111	9.6	14.5	1.0	16.5	il Desd	50		
t _{PHL}	Propagation Delay	salor2.701\18	for low pow	9.3	17.8	1.0	20.5	d consists organizer	15		
	MR to Qn LAIS O	JEDEC, SO	able in SOIC	11.8	21.1	at 0.1 Enable	1 nadw 24.0 ad	of there	50		
bas lev	bas level esion gairlo	3.3 ±0.3	segs umie hoatne	7.3	11.5	1.0	215,000,13.5	ol a ns n on ans n	15		
	9	d partormand	mic threshol	9.8	15.0	HOH 1.0 30	0 nenW17.00 s	(30) eld	50		
-	Setup Time D _n to CP	2.7	8.0		eresso up	9.5	pediance state.	ns	Pucis in		
		3.3 ±0.3	5.5		MACHINE LINE	6.5		113			
t _H	Hold Time	2.7	1.0			1.0	ie: See Section	ns of	rderii		
	D _n to CP	3.3 ±0.3	1.0			1.0					
t _{REM}	Removal Time	2.7	4.0			4.0	31	ns	s oigi		
	MR to CP angles A	MR to CP magies A	MR to CP magics/	3.3 ±0.3	2.5	75,200,0	S 28 28 £	2.5		113	
tw	Clock Pulse	2.7	8.0	- Commission	and the same	9.5	1111	ns	1		
	Width	3.3 ± 0.3	5.5		. из 🚾	6.5	0, 0, 0, 0,	0, 02 03	d b		
t _W	MR Pulse	2.7	7.5		stall 10 for	8.5		ns	31		
	Width	3.3 ± 0.3	5.0	V <	01	6.0	0.0.0.0	.0 .0 .0	30 C)-		
f _{MAX}	Maximum	2.7	55	110		45		TIT	15		
	Clock Frequency	02 00	45	60		40	40 r-erarryaut		50		
	S.C. med & J.	3.3 ±0.3	95	150		80		MHz	15		
	15 -0,		60	90	-	- 8 50			50		
toslh toshl	Output to Output Skew (Note 1)	2.7	70	mgatuso katempy (1.3	1.5		1.5	ns	50		

Note 1: Parameter guaranteed by design. toshh = |tplhm - tplhn|, toshl = |tphlm - tphln|

Capacitance

		74LVX273	74LVX273	Units
Symbol	Parameter	T _A = +25°C	T _A = TQ-QQ doisd -40°C to +85°C	
		Min Typ Max	Min Max	
CIN	Input Capacitance	4 10	10	pF
C _{OUT}	Output Capacitance	6		pF
C _{PD}	Power Dissipation Capacitance (Note 1)	31		pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per F/F)}}$



74LVX373

Low Voltage Octal Transparent Latch with TRI-STATE® Outputs

General Description

The LVX373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

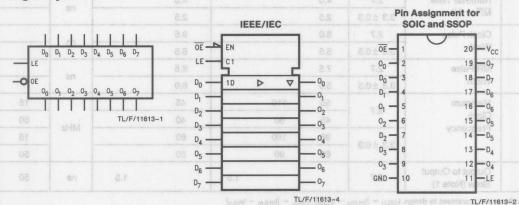
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11

Logic Symbols

Connection Diagram

Capacitance



	Pin Names	Description
Units	D ₀ -D ₇ LE OE O ₀ -O ₇	Data Inputs Latch Enable Input Output Enable Input TRI-STATE Latch Outputs

pulso numero tre pue polte por	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX373M 74LVX373MX	74LVX373SJ 74LVX373SJX	74LVX373MSCX
See NS Package Number	M20B	M20D	MSC20

- H = HIGH Voltage Level L = LOW Voltage Level
- Z = High Impedance X = Immaterial
- O₀ = Previous O₀ before HIGH to Low transition of Latch Enable

Logic Diagram

latches.

Functional Description

The LVX373 contains eight D-type latches with TRI-STATE

standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this con-

dition the latches are transparent, i.e., a latch output will

change state each time its D input changes. When LE is

LOW, the latches store the information that was present on

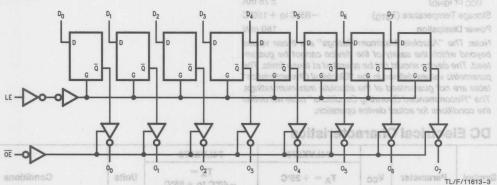
the D inputs a setup time preceding the HIGH-to-LOW tran-

sition of LE. The TRI-STATE standard outputs are con-

trolled by the Output Enable (OE) input. When OE is LOW,

the standard outputs are in the 2-state mode. When OE is HIGH, the standard outputs are in the high impedance mode

but this does not interfere with entering new data into the



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

	with the second									
		٧		1.5 2.0 2.4			1.5 2.0 2.4	2.0 3.0 3.6	High Level Input Voltage	нηV
		V	8.0 8.0 8.0		0.5 0.8 0.8			2.0 3.0 3.6	Low Level Input Voltage	
$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \mu A$	$V_{\rm IN} = V_{\rm IH}$ or $V_{\rm IL}$	V		1.9 2.9 2.48			1.8 2.9 2.58	0.S 0.0 0.8	High Level Output Voltage	
$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 m A$	V _{IVI} = V _{IIH} or V _{IL}	V	0.1 0.1 0.44		1.0 1.0 0.38	0.0		2.0 3.0 3.0	Low Level Output Voltage	Vol.
QN		Au			±0.25			3,6	TRI-STATE Output Off-State Current	
	V _{IN} = 5.5V or GN	Ац	±1.0		1.0±				Input Leakage Current	
	V _{IN} = V _{CC} or GINI	Asį						3.6	Quiescent Supply Ourrent	100

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	H	-0.5V to $+7.0V$
DC Input Diode Current (I_{IK}) $V_I = -0.5V$	1	-20 mA
DC Input Voltage (V _I)		-0.5V to 7V
DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	tovo. leve	-20 mA +20 mA
DC Output Voltage (V _O)	-0.5	V to V _{CC} + 0.5V
DC Output Source or Sink Current (I _O)		±25 mA
DC Vcc or Ground Current		

Power Dissipation 180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define

Recommended Operating Conditions Conditions

Supply Voltage (V _{CC})	2.0V to 3.6V
Input Voltage (V _I)	0V to 5.5V
Output Voltage (Vo)	emit dose shoV to Vcc
Operating Temperature (T _A)	-40°C to +85°C
Input Rise and Fall Time ($\Delta t/\Delta V$)	0 ns/V to 100 ns/V

but this does not interfere with entering new data into the

Logic Diagram

the conditions for actual device operation. DC Electrical Characteristics

(ICC or IGND)

Storage Temperature (TSTG)

				74LVX3	73	74L\	/X373	-	1	D 30	
Symbol	Parameter	Vcc	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions		
	propagation delays.	elsmiles	Min	Тур	Max	Min	Max	Auto pepty	ung al mangelin sirti terlit el	011 68001-I	
V _{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		v			
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V			
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 mA$	
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0	0.1 0.1 0.36		0.1 0.1 0.44	V	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 mA$	
loz	TRI-STATE Output Off-State Current	3.6			±0.25		±2.5	μΑ	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } G$	iND	
I _{IN}	Input Leakage Current	3.6			±0.1		±1.0	μΑ	$V_{IN} = 5.5V \text{ or GND}$ $V_{IN} = V_{CC} \text{ or GND}$		
Icc	Quiescent Supply Current	3.6			4.0		40.0	μΑ			

±75 mA

-65°C to +150°C

Symbol	Units	Parameter		V _{CC}	T _A = 25°C		Units	C _L (pF)
		-40°C to +86°C	, = +28°C		Тур	Limit		
V _{OLP}	Quiet Output Maximum	Dynamic V _{OL}	Typ Max	3.3	0.5	0.8	V	50
V _{OLV}	Quiet Output Minimum I	Dynamic V _{OL}	01 \$	3.3	-0.5	-0.8	V	50
V _{IHD}	Minimum High Level Dy	namic Input Voltage	9	3.3	tance	2.0	NOV.	50
V _{ILD}	Maximum Low Level Dy	namic Input Voltage	2.7	3.3	nod thotald	0.8	V	50

Note: Input $t_r = t_f = 3$ ns.

AC Electrical Characteristics: See Section 2 for Test Methodology

			7	74LVX37	3	74LV	X373		
Symbol	Parameter	V _{CC} (V)	T _A = +25°C				= o +85°C	Units	Conditions
			Min	Тур	Max	Min	Max		
t _{PLH}	Propagation Delay Time	2.7		7.7	15.0	1.0	18.5		$C_L = 15 pF$
tPHL	D _n to O _n			10.2	18.5	1.0	22.0	ns	$C_L = 50 pF$
		3.3 ±0.3		6.0	9.7	1.0	11.5	113	C _L = 15 pF
		0.0 10.0		8.5	13.2	1.0	15.0		$C_L = 50 pF$
t _{PLH}	Propagation Delay Time	2.7		7.5	14.5	1.0	17.5		$C_L = 15 pF$
t _{PHL}	LE to O _n			10.0	18.0	1.0	21.0	ns	$C_L = 50 pF$
		3.3 ±0.3		5.8	9.3	1.0	11.0	115	C _L = 15 pF
		0.0 _ 0.0		8.3	12.8	1.0	14.5		$C_L = 50 pF$
t _{PZL}	TRI-STATE Output Enable Time	2.7		7.7	15.0	1.0	18.5		$C_L = 15 pF, R_L = 1 ks$
t _{PZH}				10.2	18.5	1.0	22.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}$
		3.3 ±0.3		6.0	9.7	1.0	11.5	115	$C_L = 15 pF, R_L = 1 k$
		0.0 _ 0.0		8.5	13.2	1.0	15.0		$C_L = 50 \text{ pF, } R_L = 1 \text{ k}$
t _{PLZ}	TRI-STATE Output	2.7		9.8	18.0	1.0	21.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}$
t _{PHZ}	Disable Time	3.3 ±0.3	ş .	8.2	12.8	1.0	14.5	110	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}$
tw	LE Pulse Width, HIGH	2.7	6.5			7.5		ns	
		3.3 ±0.3	5.0			5.0		110	
ts	Setup Time, Dn to LE	2.7	6.0			6.0		ns	
		3.3 ± 0.3	4.0			4.0		113	
t _H	Hold Time, Dn to LE	2.7	1.0			1.0	ri maka si	ns	
		3.3 ± 0.3	1.0			1.0		113	
toslh toshl	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C _L = 50 pF

Note 1: Parameter guaranteed by design. tosch = |tplhm - tplhn|, tosh = |tphlm - tphln|

Capacitance

Capaci	tand	ce				2 for Test N	281 See Section	eristic	Charact	Noise
		74LYX373		74LVX3	73	74L	.VX373			
Symbol	Unite	Parameter AT	(V) T	A = +2	5°C		to +85°C	Units		Symbol
08	V	0.5 0.8	Min	Тур	Max	Min	Max	numixeM.	Quiet Output	Volp
CIN	Inp	ut Capacitance	2.8	4	10		10 mg	pF	Quiet Outpu	VJOV
Cout	Ou	tput Capacitance	RR	6		608	Nov turant ormetty	pF	iH muminiM	
C _{PD}	- M	wer Dissipation pacitance (Note 1)	8.8	27		age	lynamic Input Vol	lepFl w	Maximum Lo	GTIA

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

		кэтз	74LV		per Latch)	7			
Conditions	etinU	0.58+ c	T _A T — 40°C to	$T_A = +25^{\circ}C$			Vec (V)	Parameter	Symbol
		xsM	niM	xsM					
$C_L = 16 pF$			1.0				7.5	Propagation Delay Time	
$C_L = 50 \text{ pF}$	an l	22.0		18.5	10,2			D _n to O _n	
	011	11.6	1.0	9.7			8.0 ± 6.6		
Ct = 15 pF		17.5		14.5	7.5			Propagation Delay Time	14,191
Ct = 20 bE	an I				0.01			LE to On	THE
C _L = 15 pF	1 1011	11.0			8,8		8.3 ± 0.3		
$C_L = 50 \mathrm{pF}$				12.8					
$C_L = 15 \mathrm{pF}, R_L = 1 \mathrm{k}\Omega$			0.1	15.0	7.7		2.7	TRI-STATE Output	HZdj TZdj
								Enable Time	
$O_L = 16 pF, R_L = 1 k\Omega$	- 611						8.0 ± 8.8		
$C_L=50\mathrm{pF}, R_L=1\mathrm{k}\Omega$					8.5				
$C_L = 50 \mathrm{pF}, R_L = 1 \mathrm{k}\Omega$	an l		1.0				2.7	TRI-STATE Output	ters.
$C_L=50pF, R_L=1k\Omega$		14.5	1.0					Disable Time	tenz
							2.7	LE Pulse Width, RIGH	
						6.0	8.0 ± 8.8		
	en		0.0					Setup Time, D _n to LE	
			4.0			4.0	8.8 ± 0.3		
			1.0					Hold Time, Dn to LE	
							8.0 ± 8.8		
		1.5		1.6			2.7	Output to Output Skew (Note 1)	PLISON

Note 1: Parameter guaranteed by design. LOSIH = | Iputin - Iputin | LOSHL = | Iputin - Iputin |



74LVX374

Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The LVX374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

Features

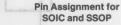
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Available in SOIC JEOEC, SOIC EIAJ and SSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance

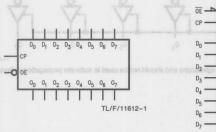
The LVX374 consists of eight edge-triggered flip-flops with

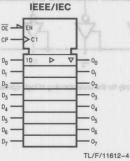
Ordering Code: See Section 11

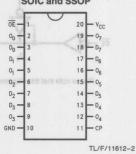
Logic Symbols

Connection Diagram









Pin Names	Description
D ₀ -D ₇ CP OE O ₀ -O ₇	Data Inputs Clock Pulse Input TRI-STATE Output Enable Input TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX374M 74LVX374MX	74LVX374SJ 74LVX374SJX	74LVX374MSCX
See NS Package Number	M20B	M20D	MSC20

Functional Description

The LVX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flipflops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

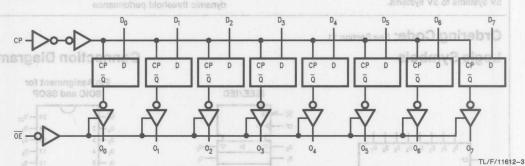
a ideal for low power/low noise 3.3V applications

Truth Table

	Inputs	i กละ อะเทากละเ ร้างกระการใกรณ	Outputs
Dn	CP	ŌĒ	On
Н	_	150	WW SHE
L		610	W. A. my las I
X	X	an Hela	All xan Z 1

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- giff (Z = High Impedance a woll beegs ripin a at AYEXV.) eriT = LOW-to-HIGH Transition = tensores principal golf

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

SSOP TYPE (SOIC EIAJ	SOIC JEDEC	
74LVX374MSCX	74LVX374SJ 74LVX374SJX	74LVX374M 74LVX374MX	Order Number
		M205	See NS Package Number

If Milit please Office	ary/Aerospa contact th Distributors	ce spe ne Nat for ava	cified o	levices ar emicondu and spec	e requir	red, ales s.	Conditi Supply Volta Input Voltage	ons ige (V _{CC}			to 3.6V
DC Inp	Voltage (V _{CC}) ut Diode Curr -0.5V ut Voltage (V _I)	ent (I _{IK})			-20 -0.5V to	mA	Output Volta Operating To	emperati	ure (T _A) ime (Δt/	-40°C to	
	tput Diode Cu = -0.5V	rrent (Id	ok)	8.8	-20	mA				Maximum Low Leve	
DC Out	= V _{CC} + 0.5V tput Voltage (\ tput Source			-0.5V to	+20 V _{CC} + 0	5V	See Senio	eoltai	acter	- t - 3 m lectrical Char	
or Si DC V _{Cl} (I _{CC} Storage	nk Current (IO C or Ground (or IGND) e Temperature	Current	1	.VX374 FA == 10 +85°C	± 75 C to +15	mA mA 0°C	$74LVX374$ $T_A = +25^{\circ}$		ooV (V)	Parameter	
Note: beyond teed. To parame	Dissipation The "Absolute I which the so The device sho etric values de	afety of ould not ofined in	the dev	rice canno ated at thes actrical Cha	t be guai se limits. aracteristi	lues ran- The ics"	9.5 11.0 6.7 9.2		7.S 3.3 ± 0.0	Propagation Delay Time CP to O _n	PLH
The "F	re not guarante commende conditions for Electrica	d Opera or actua	arting Co al device	nditions" to operation.	table will	de-8.81 0.81 6.9	7.6 10.1 5.9		2.7 3.3 ±0.5	TRI-STATE Output Enable Time	
= 1160	F. Fg 02 = 1	6		74LVX374	1.0	8874	LVX374	T	2.7	TRI-STATE Output	7 [0]
Symbol	Parameter	Vcc	Т	A = +25°	1.0		T _A = 0 C to +85°C	Units	3.3 ± 0.5	Conditions Selections	
		-	Min	Тур	Max	Min	Max	0.0	3.3 ± 0.8	Width	30
V _{IH}	High Level Input	2.0 3.0	1.5		6.5	1.5 2.0		a V	2.7 3.3 ±0.3	Setup Time Dn to CP	3
	Voltage	3.6	2.4		0.0	2.4		0.0	27	Hold Time	- 14

= 1 km	(= 50 pF, R	0		74LVX3	74 0.1	3.874	ILVX374				TATE Output		
Symbol	Parameter	Vcc		TA = +2	1.0 O°E		T _A = 0 C to +85°C		Units	3.3 ±0	Conditio	ons	
			Min	Тур	Max	Min	Max	0.	8 8.	2.7 3.3 ±0		CP PI	
V _{IH}	High Level	2.0	1.5		6.5	1.5		8.	9	7.5	Time		ts.
	Input Voltage	3.0	2.0		4.5	2.0		.5	V 8.				
			2.4		2.0	2.4		0.1	2	2.7		bloH	
V _{IL}	Low Level	2.0			0.5		0.5	0.	.S. V.				
	Input Voltage	3.0			0.8		0.8	08	V	2.7	num Clock Jeney		XAMÎ
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0	85	1.9 2.9 2.48		00	V 8.	V _{IN} =	V _{IH} or V _{IL}	I _{OH} =	= -50 μA = -50 μA = -4 mA
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0	en	0.0	0.1 0.1 0.36	1.5	0.1 0.1 0.44		A TOP		VIH or VIL TOWN	IOL =	50 μA 50 μA 4 mA
loz	TRI-STATE Output	3.6		74	±0.25		±2.5		μÁ	V _{IN} =	V _{IH} or V _{IL} = V _{CC} or GND	acita	Capa
	Off-State Current	pi	inti -		= AT				*				
I _{IN}	Input Leakage	3.6		xalf	±0.1	a	±1.0	-	μΑ		5.5V or GND		
	Current	3	iq				4 10		pur				
Icc	Quiescent	3.6	lq		4.0		40.0				V _{CC} or GND		Cour
	Supply Current		lq .						μΑ				

Noise Characteristics: See Section 2 for Test Methodology

	Conditions	ire required,	sacive	74L	VX374	Units	IS Milital
Symbol	Parameter Vonda		V _{CC} (V)	T _A =	= 25°C		C _L (pF)
V to 5,5V	Input Voltage (V _I)		-	Тур	Limit	oltage (Vo	Supply V
VOLP	Quiet Output Maximum Dynamic V _{OL}		3.3	0.5	()(10.8)	DicVe Ce	lugn 50 0
Volv	Quiet Output Minimum Dynamic VOL	Am 05-	3.3	-0.5	-0.8	V3.0-	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	V1 01 V0.0 -	3.3		2.0	Apploy	50
V _{ILD}	Maximum Low Level Dynamic Input Voltage	Arm DQ	3.3	Ol	0.8	V	50

Note: Input $t_f = t_f = 3$ ns

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVX37	1 8	74 TESE 74	LVX374		or Sink Current (Io)		
Symbol	Parameter	V _{CC} (V)	Т	A = +25°	C A	-40°	T _A = C to +85°C	Units	Conditions		
			Min	Тур	Max	Min	Max	lare	Storage Temperature (T		
t _{PLH}	Propagation	2.7		8.5	16.3	1.0	19.5	em coniver	C _L = 15 pF		
tPHL	Delay Time CP to On	2.1		11.0	19.8	1.0	23.0	ns	C _L = 50 pF		
	or to on	3.3 ±0.3		6.7	10.6	1.0	12.5	not be ap	Cp = 15 pF eff beet		
		3.3 ±0.3		9.2	14.1	1.0	16.0	ed in the	$C_L = 50 \text{ pF}$		
t _{PZL}	TRI-STATE Output	2.7		7.6	14.5	1.0	17.5	perarting	$C_L = 15 pF$, $R_L = 1 k\Omega$		
t _{PZH}	Enable Time	2.1		10.1	18.0	1.0	21.0	ctual dev	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$		
		3.3 ±0.3		5.9	9.3	1.0	11.0	ns	$C_L = 15 \text{ pF}, R_L = 1 \text{ k}\Omega$		
		3.3 ±0.3		8.4	12.8	1.0	14.5	is nativ	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$		
t _{PLZ}	TRI-STATE Output	2.7		11.5	18.5	1.0	22.0		$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$		
t _{PHZ}	Disable Time	3.3 ± 0.3	m5.1	9.6	13.2	1.0	15.0	ns	$C_L = 50 \text{ pF}, R_L = 1 \text{ k}\Omega$		
tw	CP Pulse	2.7	7.5	0.58 + 08;	3.03	8.0					
	Width	3.3 ± 0.3	5.0	Wex	nilii	5.5	qyT ni	ns			
ts	Setup Time	2.7	6.5		1.5	6.5	3	t . 0.	S level rigit Level 2		
	D _n to CP	3.3 ± 0.3	4.5		2.0	4.5	(s ns	Input 3		
tH	Hold Time	2.7	2.0		2.4	2.0		8.	s egatioV		
	D _n to CP	3.3 ± 0.3	2.0	0,5	HY.	2.0		ns o	/ _{IL} Low Level 2		
f _{MAX}	Maximum Clock	0.7	60	115		50		0.	C _L = 15 pF		
	Frequency	2.7	45 60		40		1 0	$C_L = 50 pF$			
-50 pA -50 pA	AIN OL AIF	00.100	100	160	8.1	85		MHz	C _L = 15 pF		
Am A-	F HO!	3.3 ±0.3	60	95	2.48	55	8	8 0	C _L = 50 pF		
toslh toshl	Output to Output Skew (Note 1)	2.7		1.0	1.5	0.1	0.0 1.5	ns 0	C _L = 50 pF		

Note 1: Parameter guaranteed by design. toSLH = |tpLHm - tpLHm|, toSHL = |tpHLm - tpHLm|

Capacitance V to HV = HV

	100		74LVX37	74	74LV	X374	Units	
Symbol	Parameter		A = +25	5°C	-40°C t			
	V _{IN} = 5.5V or GND	Min	Тур	Max	Min	Max		
CIN	Input Capacitance		4	10		10	pF	
C _{OUT}	Output Capacitance		6		0.6		pF	
C _{PD}	Power Dissipation Capacitance (Note 1)	Ащ	32				pF	

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{8 \text{ (per F/F)}}$

Voltage

74LVX573

Low Voltage Octal Latch with TRI-STATE® Outputs

General Description

The LVX573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs. The LVX573 is functionally identical to the LVX373 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

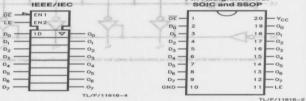
TL/F/11010-1

Features

- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
 Available in SOIC JEDEC, SOIC EIAJ and SSOP pack-
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Ordering Code: See Section 11
Logic Symbols

Connection Diagram



Pin Names	Description				
Do-D7	Data Inputs				
LE	Latch Enable Input				
OE	TRI-STATE Output Enable Input				
00-07	TRI-STATE Latch Outputs				

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE 1
Order Number	74LVX573M 74LVX573MX	74LVX573SJ 74LVX573SJX	74LVX573MSCX
See NS Package Number	M20B	M20D	MSC20

Functional Description

The LVX573 contains eight D-type latches with TRI-STATE® output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE® buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are enabled. When OE is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches. It ealer well newed well not isolat a a Available in SOIC JEDEC, SOIC EIAJ and SSOP paci

Truth Table

	bacoland	Outputs	
ŌĒ	LE	D	On
L	Н	SHCAN	VIH:
L B	H	1	T.
notsi	SIDU	X	00
Н	X	X	Z

H = HIGH Voltage

L = LOW Voltage

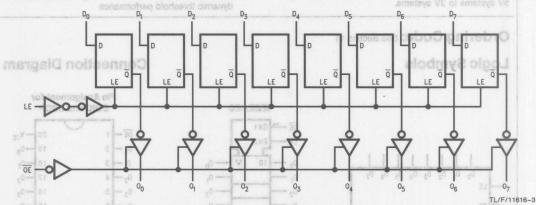
Z = High Impedance | Indoo beenga-right a at CY6XV.1 entT

mon Latch Enable (LE) and buffered colarisammE=X.rt En-

O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

package. The inputs tolerate up to 7V allowing interface of

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Description	Pln Mames
Data inputs	70-00
Letch Enable Input	
TRI-STATE Output Enable Input	EQ.
TRUSTATE Latch Outputs	-00

SBOP TYPE 1	SOIC EIAJ	SOIC JEDEC	
74LVX573MSCX	74LVX573SJ 74LVX573SJX	74LVX573M 74LVX573MX	Order Number
MSC20	M20D	M20B	See NS Package Number

P	8	٦
L	9	ŋ
	ľ	c

	oltage (V _{CC})		ryT Tyy	0.5V to +7	7.0V	Outpu	voitage (\u00e4 it Voltage	(V _O)			0	V to 5.5V
	-0.5V	(IK)	3.3 0.6	-20 MA						#Output Maxis	40°C to	+85°C
DC Input	DC Input Voltage (V _I) 0- 3.0-			-0.5V to 7V Input Rise and F			Fall Time	(Δt/Δ	(V) 0 ns	s/V to 1	00 ns/V	
	DC Output Diode Current (I _{OK})							igni olmar	CIHIV			
V _O =	-0.5V V _{CC} + 0.5V			-20 +20			ut Voltage	ani olmer	el Dyr	ve_I wo_I mumi		
	out Voltage (V _O)			to Vcc + (
DC Outp	out Source k Current (I _O)		logy	oborti ±25			08: 500	isristi		ical Cha		
	or Ground Curre				1 0	LSXA"	147					
	Temperature (T		-6	5°C to +15				201				
	issipation	Units	_ 3'88 ± 0	180				(V)			19	Symbol
	he "Absolute N which the safe					Typ	niMi					
	e device should							+	-			-
paramet	ric values defin	ed in the	e "Electrical C	Characterist	ics"	7.6						
table are	e not guarantee ecommended O	ed at the	absolute ma	ximum rati	ngs.	10.1					Do to	
the cond	ditions for actua	peraung al device	operation.	able will de	elline _{8.8}	5.9		8.0±	00			
	Gt = 50 pF		14.5	1.0	12.8							
DCE	lectrical (Chara	acteristic	CS	15.6							High
	G _L = 50 pF		0.74LVX	573	1.81 74	LVX5	73	1.5			Delay	JHG
Cumbal	Bullian O	an	12.0	25.0	1.01	r.or T _A =			-		LE to	
Symbol	Parameter	Vcc	T _A = +	25°C	-40°C to +85°C			Units	3.3	Condi	tions	
rul t - 1	13-31-0		Min Typ	Max	Min	0.7	Max	-				-
V _{IH}	High Level	2.0	1.5		1.5	-		2.7		Time	Enable	HZd
1187 - 11	Input	3.0	2.0	1.0	2.0	10.3		V				
Upl 1 = 1g	Voltage	3.6	2.4 \$1	1.0	2.4	6.1		len+	e e			
VIL	Low Level	2.0	15.5	0.5	13.2		0.5					
$R_L = 1 \log$	Input	3.0	22.0	0.8	19.1		0.8	V7.5		FATE® Output		1912
011-1	Voltage	3.6	3.31	0.8	5.01	10-1	0.8	1001	50	emiT e	Disabl	ZHd
V _{OH}	High Level	2.0	1.9 2.0	7.5	1.9			5.0	VIN	= V _{IH} or V _{IL}		= -50 μΑ
	Output Voltage	3.0	2.9 3.0		2.9			V7.9				$=-50 \mu\text{A}$
	voltage	3.0	2.58	0.8	2.48	4	5.0	8.0±	3.0		IOH =	-4 mA
VOL	Low Level	2.0	0.0	0.1			0.10.8	2.7	VIN	$= V_{IH} \text{ or } V_{IL}$		= 50 μΑ
	Output Voltage	3.0	0.0	0.1			0.18.8	EV =	3.5			50 μΑ
		3.0		0.36		and the same	0.44	1 7.5		smi	1. 1. 0. 1.	4 mA
loz	TRI-STATE Output	3.6		±0.25			±2.5	μΑ		= V _{IH} or V _{IL}		I PART
	04 044		$_{\rm JT} = V_{\rm CC}$ or G		-							
	Current	8.11	1.5		1.5			2.7		Note 1)		THEO
I _{IN}	Input Leakage Current	3.6		±0.1	- _{mulea} l =	лнаот,	±1.0	μΑ	VIN	= 5.5V or GN	D	Hote 1: Pa
lcc	Quiescent Supply Current	3.6		4.0			40.0	μΑ	VIN	= V _{CC} or GN	D	

Noise Characteristics: See Section 2 for Test Methodology (eros) 2011 5 7 munities M stulosed A

	Conditions	ire required, suctor Sales	bylces i	74L	VX573	ny/Aerost contact	ofease	
Symbol	Parameter	cifications.	V _{CC} (V)	TA	= 25°C	Units	C _L (pF)	
Vicio 5,5 Vicio 10,5 V	Input Voltage (V ₀) 0 Output Voltage (V ₀)	1.5V to +7.0V)(-/	Тур	Limit	oltage (V _C	Supply V	
VOLP	Quiet Output Maximum Dynamic VOLT philase Q	-20 mA	3.3	0.5	0.8	Van-	50	
VOLV OO	Quiet Output Minimum Dynamic VOL	-0.5V to 7V	3.3	-0.5	-0.8	VolMgs (Jugn 50	
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.3	()	2.0	ut Dyade	ghu0500	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	+ 20 mA	3.3		0.8	O V	50	

-0.5V to Voc + 0.5V

DC Output Voltage (Vo)

DC Output Source or Sink Current (Io)

Note: (Input $t_r = t_f = 3 \text{ ns}$)

AC Electrical Characteristics: See Section 2 for Test Methodology

			74	74LVX573			LVX573		DC Voc or Ground Curr	
Symbol Parameter	Parameter	V _{CC} (V)	T _A = +25°C W				T _A = C to +85°C	Units	Storage Temperature (7 Powenolithoon) Note: The "Absolute A	
			Min	Тур	Max	Min 1	onnas Maxes	y of the	beyond which the safe	
t _{PLH}	Propagation	0.7		7.6	14.5	1.0	17.5	not be a	$C_L = 15 pF$	
t _{PHL}	Delay Time	2.7		10.1	18.0	1.0	21.0 ds		C _L = 50 pF	
	D _n to O _n	00+00		5.9	9.3	1.0	11.0	ns on ns	C _L = 15 pF	
		3.3 ± 0.3		8.4	12.8	1.0	14.5	001400	$C_L = 50 \text{ pF}$	
t _{PLH}	Propagation	0.7		8.2	15.6	1.0	18.5	mara	C _L = 15 pF	
t _{PHL}	Delay Time	2.7	8	10.7	19.1	1.0	22.0		C _L = 50 pF	
	LE to On	3.3 ±0.3		6.4	10.1	1.0	12.0	ns	C _L = 15 pF	
		3.3 ±0.3	D.91	8.9	13.6	1.0	15.5		C _L = 50 pF	
t _{PZL}	TRI-STATE® Output	0.7	XSAR	7.8	15.0	1.0	18.5	2.0 2.0	C _L = 15 pF, R _L = 1 k	
t _{PZH}	Enable Time	2.7		10.3	18.5	1.0	22.0		C _L = 50 pF, R _L = 1 k	
		00.100	1	6.1	9.7	1.0	12.0	8.6	C _L = 15 pF, R _L = 1 k	
		3.3 ±0.3	0.5	8.6	13.2	1.0	15.5	2.0	C _L = 50 pF, R _L = 1 k	
t _{PLZ}	TRI-STATE® Output	2.7 ∨	8.0	12.1	19.1	1.0	22.0	3.0	C _L = 50 pF, R _L = 1 k	
tPHZ	Disable Time	3.3 ±0.3	8.0	10.1	13.6	1.0	15.5	ns	C _L = 50 pF, R _L = 1 k	
-so w	LE Pulse	2.7	6.5		0.0	7.5	0.8 0.1	ns	OH Pigin Level	
Am A-	Width	3.3 ±0.3	5.0		2.48	5.0	2,58	0.8	egalloV	
ts Au 08	Setup Time	2.7	5.01.0			5.0	0.0	2.0	OL Low Level	
50 µA	D _n to LE	3.3 ± 0.3	3.5			3.5	0.0	ns	Output	
t _H	Hold Time	2.7	1.5			1.5		0.0	200.00	
	Dn to LEIV 18' HIV = 1	3.3 ±0.3	1.5			1.5		ns	Output Output	
toshl toshh	Output to Output Skew (Note 1)	2.7			1.5		1.5	ns	C _L = 50 pF	
Note 1: F	arameter guaranteed by desi	gn. t _{OSLH} = t _P	LHm - tpLH	n, toshl	= t _{PHLm} -	t _{PHLn}].		3.6	u Input Leakage Current	
	V = Vcc or GND	gV Au	40,0			4.0		3.6	Culescent Supply Current	

Capacitance

		74LVX573			74LV		
Symbol	Parameter	T	= +2	5°C	$T_A = -40^\circ$	Units	
		Min	Тур	Max	Min	Max	
CIN	Input Capacitance		4	10		10	pF
C _{OUT}	Output Capacitance		6				pF
C _{PD}	Power Dissipation Capacitance (Note 1)		27				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr.)} = \frac{C_{PD} \times V_{CC} \times f_{|N} + I_{CC}}{8 \text{ (per latch)}}$

Capacitance

		PALVXS	LVX878 74LVX673				
Symbol Parameter		$T_{\rm A} = +25^{\circ}{\rm C}$ $T_{\rm A} = -40^{\circ}{\rm C}$ to $+85^{\circ}{\rm C}$			T _A = -40°C to +85°C		
	1000	Typ	Max			xeM	
O _{IN} Input Capacitance		4	10				Rq
Court Output Capacitance		8					PF
Capacitance (Note 1)		27					

Note 1: C_{pQ} is defined as the value of the Internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating extrent can be obtained by the equation: $\frac{C_{PD} \times V_{QO} \times I_{NI} + I_{CO}}{8 \, (por laten)}$



Section 9 Contents

8-8	LVQ Family Features
	74LVQ00 Low Voltage Quad 2-Input NAND Gate
9-7	74LVQ02 Low Voltage Quad 2-Input NOR Cate
	74LVQ04 Low Voltage Hex Inverter
9-13	74LVQ08 Low Voltage Quad 2-Input AND Gate
9-16	74LVQ14 Low Voltage Hex Inverter Schmitt Trigger Input
9-19	74LVQ32 Low Voltage Quad 2-Input OR Gate
	74LVQ74 Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop
	74LVQ86 Low Voltage Qued 2-love Sithon 2 OR Gate.
	74LVQ86 Low Voltage Quad 2-@ noitoeSQR Gate
	74LVQ138 Low Voltage 1-Vilme3-QVal tiplexer
	74LVQ138 Low Voltage 1-Vimma DV1 tiplexer 74LVQ151 Low Voltage 8-Input Multiplexer
	74LVQ157 Low Voltage Quad 2-Input Multiplexer
	74LVQ174 Low Voltage Hex D Flip-Flop with Master Reset
	74LVQ240 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
	74LVQ241 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
	74LVQ244 Low Voltage Octal Buffer/Line Driver with TRI-STATE Outputs
	74LVQ245 Low Voltage Octal Bidirectional Transceiver with TRI-STATE Outputs
	74LVQ273 Low Voltage Octal D Flip-Flop.
9-73	74LVQ373 Low Voltage Octal Transparent Latch with TRI-STATE Outputs
9-78	74LVQ374 Low Voltage Octal D Flip-Flop with TRI-STATE Outputs
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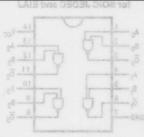


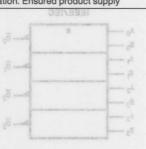


74LVQ00

LVQ Family Low Voltage Quiet CMOS Logic Control World

stures deal for low power/low noise 3.3V applications	
Features amoined blories it of omeny	Advantages
Extended V _{CC} range from 2.7V to 3.6V, compatible with Section 3.6V, compatible with Section 3.6V.	Fully characterized for unregulated battery operation
1.5 μm CMOS process enabled OA46 case-118-311 enabled gas essential and a substitution of the case-118-311	Good performance with propagation delays as fast as 9.5 ns max for octals
Low standby current (I _{CC} 40 μA max for octal over temp)	Saves power, extends battery life
± 12 mA drive current	Balanced drive, guaranteed incident wave switching into 75Ω
SOIC, EIAJ-SOIC, and QSOP (octals only) packaging	Saves board space and weight; same form between QSOP (20 leads) and SOIC (14 leads)
Alternate source available meningles A AIT	Product standardization. Ensured product supply





Description	Pin Names
Inputs	A _n , B _n
Outputs	50

	SOIC JEDEC	
74LVQ00SJ 74LVQ00SJX	74LVQ00SC 74LVQ00SCX	Order Number
M14D	ANTM	See NS Package Number





74LVQ00 Low Voltage Quad 2-Input NAND Gate

General Description

The LVQ00 contains four 2-input NAND gates.

Features

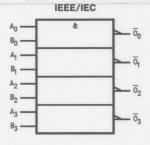
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω-8 of bi2 0 and bi2
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Logic Symbol mot emas thiglew bear some sound seval

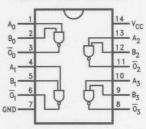
Connection Diagram , DIOS-LAIE DIOS

Pin Assignment oldalisva scruce eta mettă for SOIC JEDEC and EIAJ



TL/F/11341-1

leads) and SOIC (14 leads)



TL/F/11341-2

Pin Names	Description		
A _n , B _n	Inputs		
\overline{O}_n	Outputs		

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ00SC	74LVQ00SJ
	74LVQ00SCX	74LVQ00SJX
See NS Package Number	M14A	M14D

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (VCC) DC Input Diode Current (IIK) Guaranteed Limits -20 mA $V_1 = -0.5V$ $V_I = V_{CC} + 0.5V$ +20 mA

-0.5V to V_{CC} + 0.5V

±100 mA

DC Input Voltage (V_I) DC Output Diode Current (IOK) $V_0 = -0.5V$

0.09 -20 mA $V_0 = V_{CC} + 0.5V$ +20 mA DC Output Voltage (VO) -0.5V to $V_{CC} + 0.5V$ DC Output Source or Sink Current (Io) ±50 mA DC V_{CC} or Ground Current (ICC or IGND) ± 200 mA Storage Temperature (TSTG) -65°C to +150°C

DC Latch-Up Source or Sink Current Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaran-

teed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" the conditions for actual device operation.

Recommended Operating

Conditions

Supply Voltage (VCC) 2.0V to 3.6V Das LVQ Parameter Input Voltage (V_I) OV to VCC Output Voltage (Vo) OV to Vcc

Operating Temperature (TA) simony Community of

-40°C to +85°C

Minimum Input Edge Rate (ΔV/Δt)

3.3

AC Electrical Characteristics: See Section 2 for Test Metho

V_{IN} from 0.8V to 2.0V

MV/ns 125 mV/ns V_{CC} @ 3.0V

table are not quaranteed at the absolute maximum ratings. The trial was a supply and the absolute maximum ratings. The "Recommended Operating Conditions" table will define or yo portollive stupping (1 - n), politically a study a study of a study of the study of t

DC Characteristics

	74LVQ00	en to service of	74LV	Q00	74LVQ00		
Symbol Parameter Symbol	V _{CC} (V)	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Conditions	
	10 + 85°C		тq оТур _	Gua	aranteed Limits	Parameter	Symbol
VIH	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	8.0 2.7 8.8 ± 0.3	ationDelay	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
VOH	Minimum High Level	3.0	2.99	2.9	2.9	ration V roits	$I_{OUT} = -50 \mu\text{A}$
sn	Output Voltage	3.0	5.5	2.58	8.0 ± 2.48	V	$^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level	3.0	0.002	0.1	0,1	V	$I_{OUT} = 50 \mu A$
noiteation	Output Voltage	3.0	on delay for any t	0.36	and resource 0.44 with ord	to eula Viulces	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μА	$V_{I} = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

Conditions		QY I	Parameter	Symbol
V _{CC} = Open		4.6	Input Capacitance	CIN
Vec = 3.3V	PF		Power Dissipation Capacitance	CPD (Note 1)

DC Characteristics (Continued) TIMODOR (etc.) Spriles R mumiks M Stulozd A

		en	74L	VQ00	74LVQ00	cified do	If Military/Aerospace spendese contact the National
Symbol VD.S Parameter	V _{CC} (V)	T _A = +25°C		T _A =	Units	Conditions (20V) epilov yiqque	
nnV of VII		(oV)	Typ Guaranteed Limits			DC Input Diode Current (I _{IIC})	
I _{OLD}	†Minimum Dynamic (AT)	3.6	rating Ter	Ope	Am 05 - 36	mA	V _{OLD} = 0.8V Max (Note 1)
IOHD	Output Current	3.6	HLVG	Name of the last o	Va.0 + 5525 va.0-	mA	V _{OHD} = 2.0V Min (Note 1)
lcc an\Vm as	Maximum Quiescent Supply Current	3.6	IN from 0.8	2.0	Am 0S _ 20.0	μА (ж	V _{IN} = V _{CC} old tugtuO Od or GND V3.0 -= oV
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.6	1.0	V8.0 + 0.5V of V8.0 -	٧	(Notes 2, 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.5	-1.0	Am 08 ±	٧	(Notes 2, 3) The Content OC Voc or Ground Current
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.5	2.0	±200 mA -65°C to +150°C	٧	(Notes 2, 4) (Notes 2, 4) (Notes 2, 4) (Notes 2 Notes
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8	Arn 001±	٧	(Notes 2, 4) nemuo knië

†Maximum test duration 2.0 ms, one output loaded at a time.

beyond which the safety of the device cannot be guaran-Note 1: Incident wave switching on transmission lines with impedances as low as 75 Ω for commercial temperature range is guaranteed for 74LVQ. parametric values defined in the "Electrical Characteristics"

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND. And obtained as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) , f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol Parameter	0	74LVQ0	001	74LVQ00		74LVQ00	
	of Vcc	T _A = +25°C (V)		T _A = -40°C to +85°C C _L = 50 pF	Units		
Vour = 0.1V or Voo - 0.1V	V	2.0	Min	Тур	Max	Minadov tu Max	HIV
t _{PLH} /1.0 Propagation	n Delay	2.7 3.3 ± 0.3	2.0	8.4 7.0	13.4 9.5	2.0 siloV tuq0.0	ns
t _{PHL} Propagation	Delay	2.7 3.3 ± 0.3	1.5 1.5	6.6 5.5	11.3	1.0 12.0 1.0 8.5	ns
toshl, Output to C	utput Skew*	2.7 3.3 ± 0.3	0.1	1.0	1.5 1.5	1.5 2.1 aximum Low Level	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Leakage Current

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Oper
C _{PD} (Note 1)	PD Power Dissipation		pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.

74LVQ02 Low Voltage Quad 2-Input NOR Gate

General Description

The LVQ02 contains four, 2-input NOR gates.

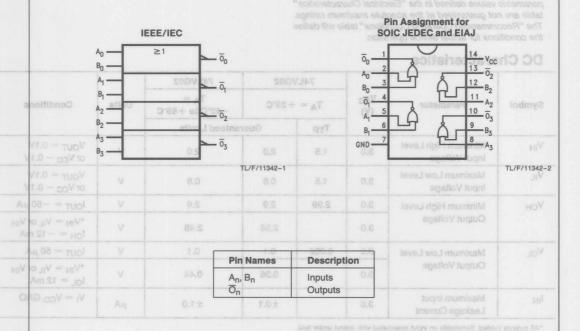
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Logic Symbol

Connection Diagram



	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ02SC	74LVQ02SJ
	74LVQ02SCX	74LVQ02SJX
See NS Package Number	M14A	M14D

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Vcc)

-0.5V to +7.0V

DC Input Diode Current (I_{IK})

 $V_1 = -0.5V$ $V_I = V_{CC} + 0.5V$

-20 mA + 20 mA

DC Input Voltage (VI) -0.5V to $V_{CC} + 0.5$ V

DC Output Diode Current (IOK)

VO = -0.5Vigs VE.E ealon wol\newcg wol not l=20 mA $V_O = V_{CC} + 0.5V$ into tiwe automatium is beginn + 20 mA DC Output Voltage (Vo) -0.5V to Vcc + 0.5V

DC Output Source and OA week nig-of-nig beeting saud #

or Sink Current (Io) ±50 mA DC V_{CC} or Ground Current DOIG DAMS 888-GTS-JIM

(ICC or IGND) Storage Temperature (TSTG)

anousoilogs eosge 200 mA -65°C to +150°C

DC Latch-Up Source or

Sink Current

 $\pm 100 \, \text{mA}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (Vcc)

2.0V to 3.6V

Logic Symbol

Input Voltage (VI)

0V to Vcc

Output Voltage (Vo)

OV to Vcc

Operating Temperature (T_A) 74LVQ

LVQ

-40°C to +85°C

Minimum Input Edge Rate (ΔV/Δt)

V_{IN} from 0.8V to 2.0V

V_{CC} @ 3.0V

125 mV/ns

DC Characteristics

	Parameter	5 ga	74L\	/Q02	74LVQ02	town of	
Symbol		V _{CC} (V)			T _A = -40°C to +85°C	Units	Conditions
	18 C A T	3	Тур	Guar	ranteed Limits		
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	٧	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	V _{OH} Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		3.0		2.58	2.48	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
V _{OL}	Maximum Low Level	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
Output Voltage	Output Voltage	3.0	Inputs	0.36	0.44	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6	Simplify	±0.1	±1.0	μА	$V_{I} = V_{CC}$, GND

^{*}All outputs loaded; thresholds on input associated with output under test.

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ02SC 74LVQ02SCX	74LVQ02SJ 74LVQ02SJX
See NS Package Numbe	M14A	MI4D

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DC Characteristics (Continued)

			74L	VQ02	74LVQ02	300	Semiconduc
Symbol Parameter	V _{CC} (V) T _A =		$T_A = +25^{\circ}C$ $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
			Тур	Gua	ranteed Limits		74LVQ04
I _{OLD}	†Minimum Dynamic	3.6	*		36	mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}	Output Current	3.6			-25	mA	V _{OHD} = 2.0V Min (Note 1)
Icc	Maximum Quiescent Supply Current	3.6	wog wol n	2.0	20.0	μΑ	V _{IN} = V _{CC} or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.6	0.1 a Guaran		٧	(Notes 2 & 3)
VOLV	Quiet Output Minimum Dynamic VOL	3.3	0.7 c	Cuaran RO.III.S		٧	(Notes 2 & 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		٧	(Notes 2 & 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

InsmnglesA nich

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Waveforms and Output Load

Symbol	AA THE	- jō		74LVQ02	-	74L	VQ02	
	Parameter	V _{CC}	T _A = +25°C C _L = 50 pF			$T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 \text{ pF}$		Units
		not see	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	2.7	1.5	6.0	10.6	1.0	12.0	
		3.3 ± 0.3	1.5	5.0	7.5	1.0	8.0	ns
t _{PHL}	Propagation Delay	2.7	1.5	6.0	10.6	1.0	12.0	
		3.3 ± 0.3	1.5	5.0	7.5	1.0	8.0	ns
toshl,	Output to Output Skew*	2.7		1.0	1.5		1.5	
toslh	Data to Output	3.3 ± 0.3		1.0	1.5		1.5	ns

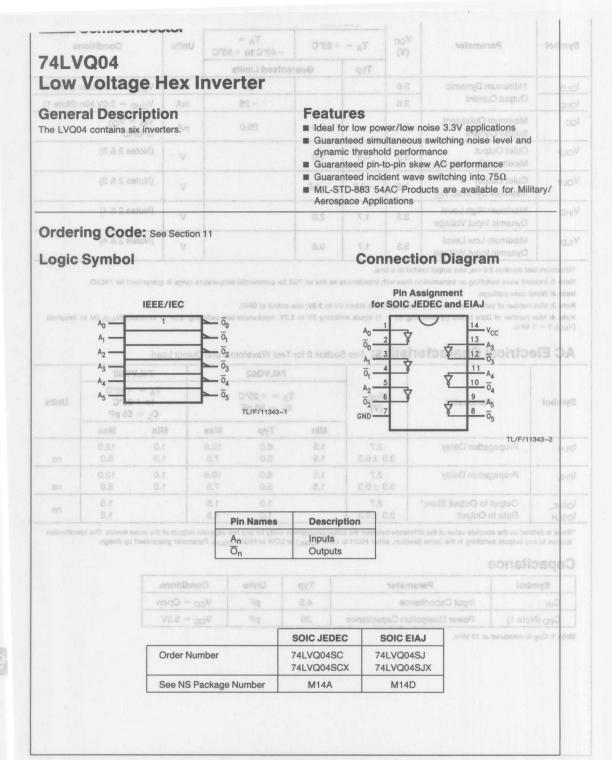
*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshi) or LOW to HIGH (toslih). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Тур	Units	Conditions	
CIN	Input Capacitance	4.5	pF	V _{CC} = Open	
C _{PD} (Note 1)	Power Dissipation Capacitance	20	pF	$V_{CC} = 3.3V$	

Note 1: CPD is measured at 10 MHz.

PWIR DIOS		
74LVQ04SJ 74LVQ04SJX	74LVQ04SC 74LVQ04SCX	Order Number
MI4D	M14A	See NS Package Number



If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	liability	and specifications. $-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK}) $V_{I} = -0.5V$ $V_{I} = V_{CC} + 0.5V$	Am	-20 mA 88 +20 mA
DC Input Voltage (VI)	Am	-0.5V to V _{CC} + 0.5V
DC Output Diode Current (I_O $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	Ащ	0.03 -20 mA +20 mA
DC Output Voltage (V _O)		-0.5V to V _{CC} + 0.5 V
or Sink Current (I _O) (I _O) DC V _{CC} or Ground Current	٧	±50 mA
(I _{CC} or I _{GND}) Storage Temperature (T _{STG})	V	±200 mA -65°C to +150°C
DC Latch-Up Source or		+100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" epison east the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating and OC Conditions

Handle Market Street		
Supply Voltage (V _{CC})	Parameter	2.0V to 3.6V
Input Voltage (V _I)		0V to V _{CC}
Output Voltage (V _O)		0V to Vcc
Operating Temperature (T	nimum Dynamic (A	OLD TMI
7/11/0	troops O to	40°C to +85°C

Minimum Input Edge Rate (ΔV/Δt)
V_{IN} from 0.8V to 2.0V

mobility criment	125 mV/ns
	mbbis criticali

Minimum Dynamic Vol

Maximum Low Level

DC Characteristics

	74LVQ04				74LVQ04		
Symbol	Parameter	V _{CC} (V)			T _A = -40°C to +85°C	Units	Conditions
Catto	CL = 80 pF		Тур	Guar	anteed Limits	100001111111111	10011170
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	v slaC noite	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
VIL	Maximum Low Level Input Voltage	0.8.0	1.5	0.8	8.0 ± 0.3	V Valido Dolar	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	Minimum High Level	3.0	2.99	2.9	8.0 ± 82.9	V	$I_{OUT} = -50 \mu A$
en	Output Voltage	0.8.5	1.0	2.58	2.48	to Cytput 5 Output	$*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
Voluntage	Maximum Low Level	3.0	0.002		the different.Oostween the		I _{OUT} = 50 μA
Output Voltage	3.0	TOTAL CO PROJECT	0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
I _{IN}	Maximum Input Leakage Current	3.6	Units	±0.1 qy	±1.0 ratem	μΑ	$V_{I} = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

PF

DC Characteristics (Continued) TIMEDOSA (GMM) SpritsA mumbksM stulpedA

			74L	VQ04	74LVQ04	ciliad de	If Military/Aerospace spe please contact the Nat
Symbol Parameter	V _{CC} (V)	T _A = +25°C		T _A = 000 - 40°C to +85°C	Units	Conditions	
no V of VO		(oV)	Тур	NO Gu	aranteed Limits		DC Input Diode Current (Ipo
I _{OLD}	†Minimum Dynamic (AT)	3.6	wating Ter	ogo	Am 05 + 36	mA	V _{OLD} = 0.8V Max (Note 1)
IOHD	Output Current	3.6	N. J.	esth a	V8.0 + 0025t V8.0-	mA	V _{OHD} = 2.0V Min (Note 1)
Icc an\Vm as	Maximum Quiescent Supply Current	3.6	in from 0.1	2.0	Am 05 – 20.0	μA	V _{IN} = V _{CC} Hadro OC or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.8	1.1	V8.0 + 00V ot V8.0-	٧	(Notes 2 & 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.8	-1.1	± 50 mA	٧	(Notés 2 & 3) UO xini2 to OCC OC OC OCCUPANT
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	± 200 mA - 65°C to + 150°C	٧	(Notes 2 & 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	Am 001 ±	V sum Rativ	(Notes 2 & 4) and And

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}) 0V to threshold (V_{IHD}) f = 1 MHz.

DC Characteristics

AC Electrical Characteristics: See Section 2 for Test Methodology

		741.700	900	74LVQ04		74LVQ04	
Symbol	Parameter 2788	V _{CC}	T _A = +25°C (V) C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF	Units
= 0.1V	TUD ^V	0.0	Min	Тур	Max	eve Min Hammi Max	HV
tpLH VI.O =	Propagation Delay	2.7	1.5	5.4	12.7	1.0 14.0	ns
	-Vva	3.3 ±0.3	1.5	4.5	9.0	1.0	'll A
t _{PHL}	Propagation Delay	2.7 93.3 ±0.3	1.5 1.5	5.4 4.5	12.0	1.0 12.0	ns
toshl, toslh	Output to Output Skew* Data to Output	2.7 3.3 ±0.3	2.58	1.0	1.5	ensileV tugh 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshil) or LOW to HIGH (toshih). Parameter guaranteed by design.

Capacitance

Symbol	Au Parameter 0.1±	Typ 1.0 1	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	CPD Power Dissipation		pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.



(IV) epsiloV hugni 74LVQ08 **Low Voltage Quad 2-Input AND Gate** 40°C to +85°C

General Description

The LVQ08 contains four, 2-input AND gates.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Absolute Maximum Ratings (Note) If Military/Aerospace specified devices are required, Office/Distributors for availability and specifications.

Supply Voltage (Voc)

TL/F/11344-2

Ordering Code: See Section 11

IEEE/IEC

&

00

- 0,

- 02

- 03

Logic Symbol

A1 .

A2

B2 .

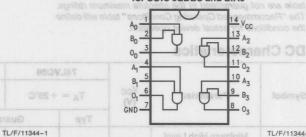
A3 .

lour = -50 µA "VIN = VIL OF VIN Amst - = Hol

HIV TO JIV = MIV lot = 12 mA VI = VCC. GND

Connection Diagram

Pin Assignment for SOIC JEDEC and EIAJ



2.48		
0.1	Pin Names	Description
	A _n , B _n	Inputs
0.44	On 80.0	Inputs Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ08SC 74LVQ08SCX	74LVQ08SJ 74LVQ08SJX
See NS Package Number	M14A	M14D

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) DC Input Diode Current (IIK) -0.5V to +7.0V

 $V_1 = -0.5V$

-20 mA +20 mA

 $V_{I} = V_{CC} + 0.5V$ DC Input Voltage (Vi)

-0.5V to $V_{CC} + 0.5V$

DC Output Diode Current (IOK)

Vo = 0.5V qs VS.8 esion wol\newood wol not 1=20 mA Vo = Vcc + 0.5Vninotive audenatiumie beetner+20 mA

DC Output Voltage (VO) -0.5V to VCC + 0.5V

Guaranteed pin-to-pin skew AC pe

DC Output Source or Sink Current (Io)

DC Voc or Ground Current (ICC or IGND)

Am 200 ± 200 mA

Storage Temperature (TSTG)

-65°C to +150°C

DC Latch-Up Source or

Sink Current

±100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (VCC) IVO

2.0V to 3.6V

Input Voltage (V_I)

OV to Vcc

Output Voltage (VO) Operating Temperature (T_A) OV to Vcc

74LVQ

-40°C to +85°C

Minimum Input Edge Rate (ΔV/Δt) Δ [21909]

Ordering Code: See Section 11

Logic Symbol

V_{IN} from 0.8V to 2.0V

DC Characteristics

	10 As	A ₁ —	74L	VQ08	74LVQ08	the second of	
Symbol	Parameter Parameter	V _{CC} (V)	T _A =	+25°C	T _A = -40°C to +85°C	Units	Conditions
60	- UND	Тур	Guar	ranteed Limits	t		
YEI NAVIT	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
	Output Voltage	3.0		2.58	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level	3.010	0.002	0.1	mi9 0.1	V	$I_{OUT} = 50 \mu A$
	Output Voltage	3.0	Inputs Outputs	0.36	nO 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μА	$V_{I} = V_{CC}$, GND

^{*}All outputs loaded; thresholds on input associated with output under test.

SOIC EIAJ	SOICJEDEC	
74LVQ08SJ 74LVQ08SJX	74LVQ08SCX 74LVQ08SCX	Order Number
M14D	W14A	See NS Package Number

DC Characteristics (Continued)

			74L	VQ08	74LVQ08	74LVQ08	
Symbol	Parameter	V _{CC} (V)	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Conditions
			Тур	Gua	ranteed Limits		ZALVQ14
I _{OLD}	†Minimum Dynamic	3.6	331(11)	108 11	36	mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}	Output Current	3.6		a strip	-25	mA	V _{OHD} = 2.0V Min (Note 1)
Icc	Maximum Quiescent Supply Current	3.6	wod wol s	2.0	filmdo 20.0 hw nose	а µА	V _{IN} = V _{CC} or GND
V _{OLP}	Quiet Output Maximum Dynamic VOL	3.3	0.4	0.8	ed, jitter-fræ output noise margin than	uplyytetin a greats	(Notes 2 & 3) ugni grigners
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	8.0-8	line gnlog-evilised		(Notes 2 & 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0	nd is essentially in- lage variations.	3 20 (A) 10	(Notes 2 & 4) natri benime bna erutaregnat of avillena
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8		V	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ. Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n = 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) , f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

	125	12-1		74LVQ08	10-00	THE RESERVE OF THE PARTY OF	/Q08	
Symbol	Parameter	V _{CC} (V)		T _A = +25°C C _L = 50 pF	20-02 20-02	to +	-40°C 85°C 50 pF	Units
	- Sandanananananananananananananananananan	GNO CHO	Min	Тур	Max	Min	Max	
tplH S-84611	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	9.0 7.5	13.4 9.5	1.0	14.0 10.0	ns
t _{PHL}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	8.4 7.0	12.0 8.5	1.0	13.0 9.0	ns
toshl, toslh	Output to Output Skew*	2.7 3.3 ±0.3		1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	17	pF	$V_{CC} = 3.3V$

Note 1: CPD is measured at 10 MHz.

		SOIC EIAJ
	74LVQ14SC 74LVQ14SCX	
See NS Package Number		



74LVQ14

Low Voltage Hex Inverter with Schmitt Trigger Input

= AT

40°C to +85°C

General Description

The LVQ14 contains six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The LVQ14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

1.8

 MIL-STD-883 54AC products are available for Military/ Aerospace applications

DC Characteristics (Commund)

Symbol

THEO

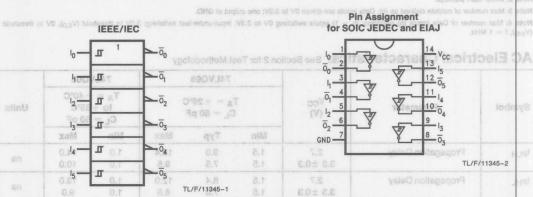
Capacitance

Ordering Code: See Section 11

le outguts of the same device. The specification

Logic Symbol

Connection Diagram



la spé	Pin Names	Description
9.	LOW to HIGH (ton WOLL)	Inputs of HOIH
	Ōn	Outputs

Truth Ta	ible sinti	Typ	Parameter	
V _{pC} = Open	Input Rq	Output	Input Capacitance	
$V_{QC} = 3.3 V$	A an	Ō	Power Dissipation	G90
	L	Н	Capacitance	
	н	L	t at 10 MHz.	

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ14SC	74LVQ14SJ
	74LVQ14SCX	74LVQ14SJX
See NS Package Number	M14A	M14D

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office /Distributors for availability and enecifications

Office/Distributors for ava		and specifications.
Supply Voltage (V _{CC})	asinu	-0.5V to +7.0V
DC Input Diode Current (I_{IK}) $V_I = -0.5V$		-20 mA
$V_1 = V_{CC} + 0.5V = AT$	V	9.1 + 20 mA
DC Input Voltage (V _I)		-0.5V to V _{CC} + 0.5V
DC Output Diode Current (I_C $V_C = -0.5V$	K) Am	8€ −20 mA
$V_O = V_{CC} + 0.5V$		+20 mA
DC Output Voltage (V _O)		-0.5 V to to $V_{CC} + 0.5$ V
or Sink Current (I _O)	Ац	0.09 ±50 mA
DC Vcc or Ground Current		

Sink Current ±100 mA Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define

the conditions for actual device operation.

Recommended Operating and OC Conditions

Supply Voltage (V _{CC})	Parameter	2.0V to 3.6V
Input Voltage (V _I)		0V to V _{CC}
Output Voltage (V _O)		0V to V _{CC}

Operating Temperature (TA) 0.0 N

C to +85°C	-40°C Θ (ΔV/Δt)	Edge Rate	74LVQ Vinimum Input
125 mV/ns	†Minimum Dynamic Output Current	V to 2.0V	V _{IN} from 0.8 V _{CC} @ 3.0V
аног		3.6	.00 = 0.01
	Maximum Quiescent - Supply Current	3.6	
AOPA	Quiet Output Maximum Dynamic Vot	3.3	e.o
ATOA	Quiet Output		

Note 1: incident wave switching on

Note 1: Cpp is measured at 10 MHz.

DC Characteristics

(ICC or IGND)

Storage Temperature (TSTG)

DC Latch-Up Source or

DIORISONO OT	ing: s.av to toreshold (vil.p), ov		74L	VQ14	NS SWAJIN I	74LVQ14	in) exogni saac	(Virib), t = 1 MHz.	
Symbol Parameter		V _{CC}	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions	
	781.VQ14		Тур	Gua	aranteed	Limits			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9		2.9	₁Vems	$I_{OUT} = -50 \mu\text{A}$	
	Min Max	3.0	Ma	2.58	114	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$	
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	1.5	0.9 = 8.8	V	$I_{OUT} = 50 \mu\text{A}$	
an	1.5 18.0	3.0	1.17	0.36	a.t	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
IIN	Maximum Input Leakage Current	3.6	1.5	D.F ±0.1		£1.0 8.6	μA	VI = VCC, GND	
V _{t+olitosqs}	Maximum Positive Threshold	3.0	n delay for any r LOW to HIGH	2.2	veen the are er HIGH to	vied2.2 energible erir i edite , no toenb emaa	soluty alue of	T _A = Worst Case	
V _t -	Minimum Negative Threshold	3.0		0.5		0.5	V	T _A = Worst Case	

±200 mA

-65°C to +150°C

Parameter *All outputs loaded; thresholds on input associated with output under test. Symbol

Symbol	Parameter	V _{CC} (V)	TA=	+ 25°C	T _A = -40°C to +85°C	Units	Conditions	
DOV of V		(oV)	Typ Guaranteed Limits				DC Input Diode Current (IIK)	
V _{h(max)}	Maximum Hysteresis	3.0	rating Ten	1.2	Am 0S+ 1.2	٧	T _A = Worst Case	
V _{h(min)}	Minimum Hysteresis	3.0	mum Inpu	0.3	Va.0 + 0.3 Va.0 -	٧	T _A = Worst Case	
I _{OLD}	†Minimum Dynamic	3.6	N from 0.6	4	Am 05 — 36	mA	V _{OLD} = 0.8V Max (Note 1)	
I _{OHD}	Output Current	3.6	AC.0 0 30		Am 05 + -25	mA	V _{OHD} = 2.0V Min (Note 1)	
Icc	Maximum Quiescent Supply Current	3.6		2.0	20.0	μА	V _{IN} = V _{CC} or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.9	1.1	Am oos±	٧	(Notes 2, 3) 10 10 00 V OC	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.8	-1.1	-95°C to +150°C	٧	(Notes 2, 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.9	2.0	gs" are those values as cannot be guarar-	helv mu	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.3	2.0	ed at these limits. The thical Characteristics'	No Operal	(Notes 2, 4)	

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}) , 0V to threshold (V_{IHD}) , f = 1 MHz.

Parameter

AC Electrical Characteristics: See Section 2 for Test Methodology

		atimi.) b		74LVQ14	Typ	74LV	/Q14	
Symbol	Parameter	V _{CC} (V)		T _A = +25 C _L = 50 p		$T_A = -40^{\circ}$ $C_L =$	C to +85°C 50 pF	Units
VIL or VIH	= NIA,	84.5	Min	ва тур	Max	Min	Max	
t _{PLH}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	11.4 9.5	19.0 13.5	1.5 1.5 J wo.	21.0 15.0	ns
tPHL HIV 10 JIV	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	9.0 7.5	16.2 11.5	1.5 1.5	19.0 13.0	ns
toshl, toslh	Output to Output Skew* Data to Output	2.7 3.3 ± 0.3		1.0 1.0 ± 1.0	1.5 1.5		1.5 6.1 xianum l Leekage O	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	20	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.

74LVQ32 **Low Voltage Quad 2-Input OR Gate**

General Description and Jugal muminiM

The LVQ32 contains four, 2-input OR gates.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required. places contact the National Semiconductor Sales Office/Distributors for availability and apacifications.

Features

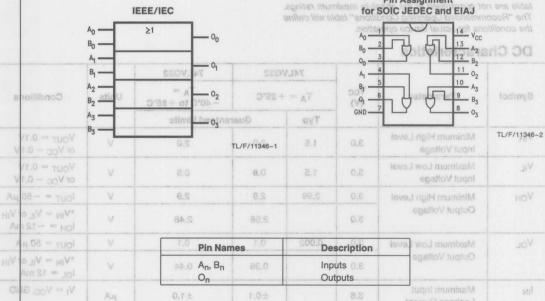
- ▲ Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dyva namic threshold performance (ov) epstlov tuctuo od
 - Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Logic Symbol

Connection Diagram T : 10/4 annot be guaran-

Pin Assignment



	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ32SC	74LVQ32SJ
	74LVQ32SCX	74LVQ32SJX
See NS Package Number	M14A	M14D

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})

-0.5V to +7.0V

DC Input Diode Current (IIK)

 $V_1 = -0.5V$ $V_I = V_{CC} + 0.5V$ -20 mA +20 mA

DC Input Voltage (V_I)

-0.5V to $V_{CC} + 0.5V$

DC Output Diode Current (IOK)

VO = -0.5V as VS.S ealon walkiewog wal tot le-20 mA VO = VCC + 0.5V dative superaturals besture + 20 mA

DC Output Voltage (Vo) -0.5V to to Vcc + 0.5V

DC Output Source

or Sink Current (IO) # ±50 mA

DC V_{CC} or Ground Current Day OAA3 083-018-118 anollacilique ecsada ± 200 mA

(ICC or IGND) Storage Temperature (TSTG)

-65°C to +150°C

DC Latch-Up Source or

Sink Current

±100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (VCC)

LVQ

2.0V to 3.6V

Input Voltage (V_I)

OV to VCC OV to VCC

Output Voltage (Vo) Operating Temperature (T_A)

-40°C to +85°C

Logic Symbol

Minimum Input Edge Rate (ΔV/Δt)

V_{IN} from 0.8V to 2.0V

VCC @ 3.0V

74LVQ

DC Characteristics

	11/10/	14	74L	VQ32	74LVQ32										
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions								
	0-2-1	010	Тур	Guar	anteed Limits	- th									
VIH	Minimum High Level Input Voltage	3.0	3.0 1.5 2.0 2.0		3.0 1.5 2.0 2.0		3.0 1.5 2.0 2.0		3.0 1.5 2.0 2.0 V		3.0 1.5 2.0 2.0		1.5 2.0 2.0		$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	٧	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$								
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$								
	Output Voltage	3.0		2.58	2.48	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$								
V _{OL}	Maximum Low Level	3.0	0.002	0.1	maté pag 0.1	V	$I_{OUT} = 50 \mu A$								
Output Voltage		3.0	igni tuCi	0.36	n∃ nA 0.44	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$								
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μΑ	$V_{I} = V_{CC}$, GND								

^{*}All outputs loaded; thresholds on input associated with output under test.

BOIC EIAJ	SOIC JEDEC	
74LVQ32SJ 74LVQ32SJX	74LVQ32SC 74LVQ32SCX	Order Number
	MIAA	See NS Package Number

Symbol	Parameter	V _{CC} (V)			Units	Conditions	
			Тур	Gua	ranteed Limits		74LVQ74
lold	†Minimum Dynamic	3.6		eville	36	mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}	Output Current	3.6			-25	mA	V _{OHD} = 2.0V Min (Note 1)
Icc	Maximum Quiescent Supply Current	3.6	duqni suor	2.0	20.0	μΑ	$V_{IN} = V_{CC}$ or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	(3.3	0.5	0.8	with Asynchronous ary (Q. Q) outputs.	flip/lop-	(Notes 2 & 3)
V _{OLV}	Quiet Output Minimum Dynamic VOL	3.3	-0.5	-0.8	the outputs on the iggening occurs at a	staned in e. CVok t	(Notes 2 & 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1,9	2.0	ng pulse. After the	elthy-goir oftage ha	(Notes 2 & 4) notinement and color learning and col
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.899	0.8	present will not be t rising edge of the	rotermation to Vity Item	(Notes 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package. In the property OAAS 589-072-184 in

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V: Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

	in illustration and annual			74LVQ32		74L\	/Q32	orgo.
Symbol Parameter	Pin Assignment			T _A = +25°C C _L = 50 pF		$T_A = -40^{\circ}C$ $to + 85^{\circ}C$ $C_L = 50 pF$		Units
	The second second	Min	Тур	Max	Min	Max		
t _{PLH}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	8.4 7.0	12.7 9.0	1.5	14.0 10.0	ns
t _{PHL}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	8.4 7.0	12.0 8.5	1.0 1.5	13.0 9.0	ns
toshl,	Output to Output Skew*	2.7 3.3 ±0.3		1.0	1.5 1.5	0 0 00	1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshi) or LOW to HIGH (toshi). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Oper
C _{PD} (Note 1)	Power Dissipation Capacitance	Direct Fleer In	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.

	33GBL 3108	SOIC EIAJ
Order Number	74LVQ748C 74LVQ748CX	74LVQ74SJ 74LVQ74SJX
See NS Package Number	M14A	M14D



74LVQ74

Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

40°C to +85°C

General Description

The LVQ74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \overline{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW input to \overline{S}_D (Set) sets Q to HIGH level LOW input to \overline{C}_D (Clear) sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q}_D

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/
 Aerospace applications

Ordering Code: See Section 11

Logic Symbols

AC Electrical Characteristics: See Section 2 for Test Methodology AC Electrical Characteristics: See Section 2 for Test Methodology

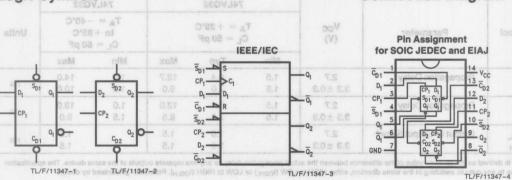
DC Characteristics (Continued)

Maximum High Level

Symbol

 $(V_{HH}V)$, f = 1 MHz.

Symbol



		3	apacitance.
Pin Names	Description	Parameter	Symbol
D ₁ , D ₂ CP ₁ , CP ₂	Data Inputs Clock Pulse Inputs	Input Capacitan	CIN
$\overline{C}_{D1}, \overline{C}_{D2}$ $\overline{S}_{D1}, \overline{S}_{D2}$	Direct Clear Inputs Direct Set Inputs	Power Dissipati Capacitance	Cpp (Note 1)
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs	at 10 MHz.	late 1: Cpg is measured

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ74SC	74LVQ74SJ
	74LVQ74SCX	74LVQ74SJX
See NS Package Number	M14A	M14D

Truth Table	(Each Half)			(atol/		ite Maximum Ra	
		suom	Inputs	Outp		/Aerospace specified doniset the National S	
2.0V to 3.6V 6V to V _{GG} 0V to V _{GG} -40°C to +85°C 125 mV/ns	(A) (AV/AQ)	H H H H H H = HIGH VC L = LOW Vol X = Immateri	Itage Level al to-HIGH Clock Tr	X H X L X H H H L X Q ₀	H H L Q ₀	C + 0.5V oftage (V _I) Diode Current (I _{OK}) 0.5V CC + 0.5V Voltage (V _O) Source	Supply Vol. Supply Vol. V ₁ = -0 V ₂ = -0 V ₃ = -0 OC Input V ₄ V ₆ = -0 OC Output V ₆ = -0 OC Output V ₇ V ₇ = -0 OC Output V ₈ OC Output V ₉ OC Output V ₉
Logic Diagra \bar{s}_{p}	am			Am 00\$±		Ground Current swo) impersture (Tsrg) Up Source or	
CP —	->-) [able are not
c _D	alinU	- 40°C to + 65°C seed Limits	(Supremont)	Typ	(V)	Peramote	lodmy
VI Please note that	t this diagram is p				should not be	used to estimate propagation dela	rL/F/11347- ys.
$V_{OUT} = 0.1V$ or $V_{OO} = 0.1V$	V		8.0		3.0	Maximum Low Level Input Voltage	
10UT = -50 HA				2.99			
$V_{\rm II} = V_{\rm II}$ or $V_{\rm II}$					3.0		
lour = 50 µA				900,0	3.0		
$^{*}V_{iN} = V_{iL} \text{ or } V_{iR}$ $j_{OL} = 12 \text{ mA}$			0.36				
VI = VCC, GND		0.1±				Maximum input Leakage Current	M

*All outputs loaded; thresholds on input associated with output under test.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Output Diode Current (I_{OK})

 $V_{\rm O} = -0.5 {\rm V}$ $-20 {\rm mA}$ $V_{\rm O} = {\rm V}_{\rm CC} + 0.5 {\rm V}$ $+20 {\rm mA}$ DC Output Voltage (V_O) $-0.5 {\rm V}$ to to ${\rm V}_{\rm CC} + 0.5 {\rm V}$

DC Output Source

or Sink Current (I_O) #550 to notional H±50 mA

DC V_{CC} or Ground Current

 $(I_{CC} \text{ or } I_{GND})$ $\pm 200 \text{ mA}$ Storage Temperature (T_{STG}) $-65^{\circ}\text{C to} + 150^{\circ}\text{C}$

DC Latch-Up Source or

Sink Current ± 100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteritics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating de Taturi Conditions

Supply Voltage (V_{CC})

L = LOW Voltage Leval

 LVQ
 2.0V to 3.6V

 Input Voltage (V_I)
 0V to V_{CC}

 Output Voltage (V_O)
 0V to V_{CC}

Operating Temperature (T_A) 74LVQ

-40°C to +85°C

Logic Diagram

Minimum Input Edge Rate ($\Delta V/\Delta t$)

V_{IN} from 0.8V to 2.0V

V_{CC} @ 3.0V 125 mV/ns

DC Characteristics

0	-60 F	1-0	74L	VQ74	74LVQ74	0<1-	
Symbol	Parameter	V _{CC} (V) T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions	
	Destacement	THE RESERVE	Тур	Guar	anteed Limits		g ²
V _{IH}	Minimum High Level	3.0	1.5	2.0	2.0	this degram is	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	٧	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$
	Output Voltage	3.0		2.58	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
V _{OL}	Maximum Low Level	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
	Output Voltage	3.0		0.36	0.44	V	$^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μΑ	$V_{I} = V_{CC}$, GND

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued) SlobortieM test not a noticed see a 1811 mentiupe A gnits required DA

	74LV074	174	74LV	Q74	74LVQ74				
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions		
	C _L = 50 pF	114 1	Тур	Gu	aranteed Limits				
lold	†Minimum Dynamic	3.6	dÅ		36	mA	V _{OLD} = 0.8V Max (Note 1)		
I _{OHD}	Output Current	3.6	8,1		7.S -25 WOJ	mA	V _{OHD} = 2.0V Min (Note 1)		
lcc en	Maximum Quiescent Supply Current	3.6	2.4	2.0	7.2 20.0 WO	г юди	V _{IN} = V _{CC} or GND		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.2	0.8	2.7	٧	(Notes 2 and 3)		
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	(3.3	-0.2	-0.8	2.7	Vemi	(Notes 2 and 3)		
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	001 0.0	٧	(Notes 2 and 4)		
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	ewY -	V	(Notes 2 and 4)		

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ. CPD

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (VILD, 0V to threshold $(V_{IHD}, f = 1 MHz.$

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVQ74		74L	VQ74	
Symbol	Parameter	V _{CC} (V)				T _A = to + C _L =	Units	
			Min	Тур	Max	Min	Max	
f _{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	50 100	100 125		40 95		MHz
t _{PLH}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n	2.7 3.3 ± 0.3	3.5 3.5	9.6 8.0	16.9 12.0	3.5 2.5	19.0 13.0	ns
t _{PHL}	Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n	2.7 3.3 ±0.3	4.0 4.0	12.6 10.5	16.9 12.0	3.5 3.5	19.0 13.5	ns
t _{PLH}	Propagation Delay CP_n to Q_n or \overline{Q}_n	2.7 3.3 ±0.3	4.5 4.5	9.6 8.0	19.0 13.5	4.0 4.0	23.0 16.0	ns
t _{PHL}	Propagation Delay CP_n to Q_n or \overline{Q}_n	2.7 3.3 ±0.3	3.5 3.5	9.6 8.0	19.7 14.0	3.5 3.5	21.0 14.5	ns
toshl, toslh	Output to Output Skew* Data to Output	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology (1997) 2011219 2012 10 2012

		74LV074	\$10V.J\$174LV	274	74LVQ74	
Symbol	Parameter	AT VCC (V)	C _L = 5	25°C 0 pF	T _A = -40°C to +85°C C _L = 50 pF	
(LetoW) vsM	/8.0 ≈ n roV Arn	16	Тур	Guaran	teed Minimum	030
(Nowest)	Set-up Time, HIGH or LC	2.7 3.3 ±0.3	1.8 1.5	5.0 4.0	4.5	ns
t _H	Hold Time, HIGH or LOV D _n to CP _n	V 00 2.7 3.3 ±0.3	-2.4 -2.0	0.5 0.5	0.5 years	ns
t _W	Pulse Width	2.7 3.3 ±0.3	3.6 9.0	7.0 5.5	10.0 7.0	ns
t _{rec}	Recovery Time	2.7 3.3 ±0.3	3.0	0	Minimum Oynamic V	ns

Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	25	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz. 18.8 grandolive tent-reconstruction. Veloc of V0 predictive stugal (1 - it) predictive (in) shoot shoot by addition with the about

AC Electrical Characteristics: See Section 2 for Test Mathodology

1076	24LV		74LV074				
TA = -40°C to +86°C CL = 50 pF		Vcc TA = +25°C to +85°C				Symbol	
			Typ	niM			
	40 95		100		2.7 3.8 ±0.8	Maximum Glock Frequency	max
19.0	3.5 2.5	16,9	8.0 0.8	3.5 3.5	2.7 3.3 ± 0.8	Propagation Delay Con or Son to On	
19.0	3.6 8.5	16,9		4.0	2.7 3.3 ± 0.3	Propagation Delay Con or Spn to Qn	
23.0	4.0			4.5 4.5		Propagation Delay. CP_n to Q_n or \overline{Q}_0	
21.0				3.5	2.7 3.3 ± 0.3	Propagation Dalay CP _n to O _n or \overline{O}_n	THAI
1.6 1.6					2.7 3.3 ± 0.3	Output to Output Skew* Data to Output	

"Skow is defined as the absolute value of the difference between the adual propagation delay for any two separate caputa of the same device. The stapping to the same direction, sitter HICH to LOW (togas) or LOW to HICH (togas). Perameter guaranteed by design.

74LVQ86 Low Voltage Quad 2-Input Exclusive-OR Gate

General Description and Jugat muminiM

The LVQ86 contains four, 2-input exclusive-OR gates.

Features

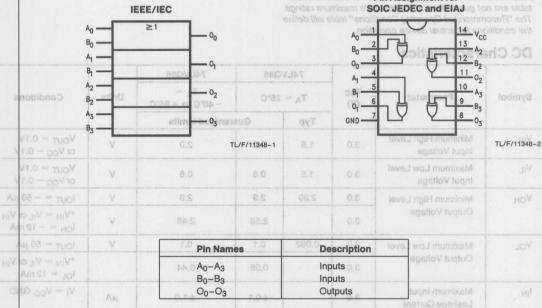
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC Products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Logic Symbol

soules each Connection Diagram of solid response admired the granter of the devices cannot be solid to the devices cannot be

Pin Assignment for



	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ86SC 74LVQ86SCX	74LVQ86SJ 74LVQ86SJX
See NS Package Number	M14A	M14D

V _O = V _{CC} + 0.5V DC Output Voltage (V _O) DC Output Source or Sink Current (I _O) DC V _{CC} or Ground Current (I _{CC} or I _{GND})	+ 20 mA - 0.5V to V _{CC} + 0.5V - 20 mA + 20 mA - 0.5V to V _{CC} + 0.5V ± 50 mA ± 200 mA	Input Voltage (V _I) Output Voltage (V _O) Operating Temperature (T _A) 74LVQ Minimum Input Edge Rate (ΔV/Δt) V _{IN} from 0.8V to 2.0V V _{CC} @ 3.0V
Storage Temperature (T _{STG})	-65°C to +150°C	

±100 mA

2.UV TO 3.6V OV to VCC OV to VCC 40°C to +85°C

125 mV/ns

Ordering Code: See Section 11

Logic Symbol

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Characteristics

DC Latch-Up Source or Sink Current

	Parameter	Barrer A	74LVQ86 74LVQ86 VCC (V) TA = 25°C TA = -40°C to +85°C		74LVQ86		
Symbol						Units	Conditions
	20-3-4	Zone GND	Тур	Gua	ranteed Limits	1	
VIH	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	٧	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
	Output Voltage	3.0		2.58	2.48	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level	3.0	0.002	0.1	0.1	٧	$I_{OUT} = 50 \mu A$
	Output Voltage	3.0	igni mat	0.36	A-0A 0.44		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6	ijo Ou	±0.1	€O-00±1.0	μΑ	$V_{I} = V_{CC}$, GND

^{*}All outputs loaded; thresholds on input associated with output under test.

BORD EIAJ	
74LVQ868J 74LVQ86SJX	Order Number
	See NS Package Number

DC Characteristics (Continued)

			74L	VQ86	74LVQ86	703	ALAN Semicondud	
Symbol Parameter	Parameter	V _{CC} (V)	A = 25°C		T _A = -40°C to +85°C	Units	Conditions	
	25 m# co	Тур	Gua	ranteed Limits		74LVQ125		
IOLD	†Minimum Dynamic	3.6	N 1 6	10000	36	mA	V _{OLD} = 0.8V Max (Note 1)	
IOHD	Output Current	3.6	70 FAN	Eogla	-25	mA	V _{OHD} = 2.0V Min (Note 1)	
Icc	Maximum Quiescent Supply Current	3.6	r low pow	2.0	-hud p20.0 mi-non	μΑ	$V_{IN} = V_{CC}$ or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.5	0.8		٧	(Notes 2, 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.5	-0.8		٧	(Notes 2, 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0		٧	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.8	0.8		V	(Notes 2, 4)	

†Maximum test duration 20 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (VILD), 0V to threshold

AC Electrical Characteristics: See Section 2 for Test Methodology

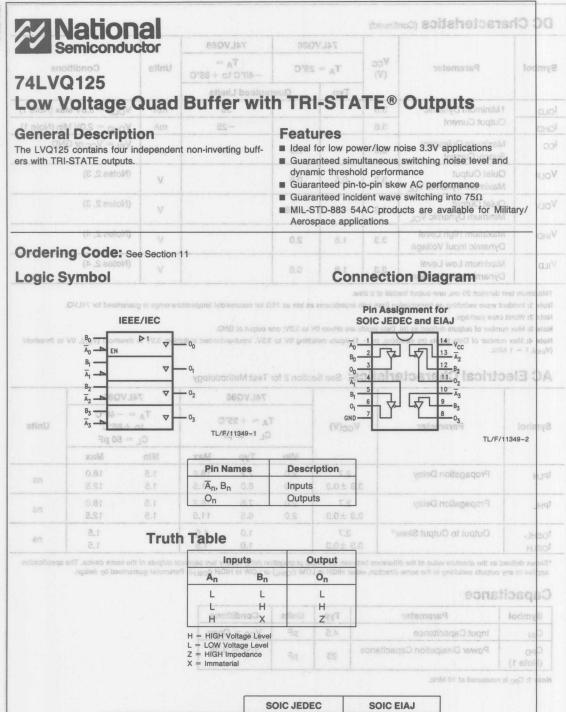
Symbol 8-866	Symbol Parameter V		T _A = $+25^{\circ}$ C		c e	74L' T _A = to + C _L =	Units		
			p	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	2.7 3.3 ±0.3	2.0	7.2 6.0	16.2 11.5	1.5 1.5	18.0 12.5	ns	
t _{PHL}	Propagation Delay	2.7 3.3 ±0.3	2.0 2.0	7.8 6.5	16.2 11.5	1.5 1.5	18.0 12.5	ns	
toshl,	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5	Burt	1.5 1.5	ns	

*Skews defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	23	pF	$V_{CC} = 3.3V$

Note 1: CPD is measured at 10 MHz.



	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ125SC 74LVQ125SCX	74LVQ125SJ 74LVQ125SJX
See NS Package Number	M14A	M14D

Office/Distributors for available Supply Voltage (V _{CC}) DC Input Diode Current (I _{IK}) $V_{I} = -0.5V$ $V_{I} = V_{CC} + 0.5V$		-0.5V to +7.0V -20 mA +20 mA	Gu Gu	Supply Voltage LVQ Input Voltage (Output Voltage Operating Ten 74LVQ	(V _I) ∋ (V _O)	thinimum Dynamic (AT) e	0.0V to 3.6V 0V to V _{CC} 0V to V _{CC} C to +85°C
DC Input Voltage (V_I) DC Output Diode Current (I_O $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O)	K) Au	-0.5V to V _{CC} + 0.5V -20 mA +20 mA -0.5V to to V _{CC} + 0.5V	4.0		t Edge R 3V to 2.0	Rate (ΔV/Δt)	125 mV/ns
DC Output Source or Sink Current (I _O)	V	± 50 mA		a.o		Quiet Output Minimum Dynamic Vol.	
DC V _{CC} or Ground Current (I _{CC} or I _{GND}) Storage Temperature (T _{STG})	٧	±200 mA -65°C to +150°C		1.7	8.8	Maximum High Level Dynamic Input Voltage	
DC Latch-Up Source or Sink Current	٧	±100 mA		a.t	3.8	Maximum Low Level Dynamic Input Voltage	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteritics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Characteristics

	74FAF1352		74LVQ125		74LVQ125			
Symbol	Parameter	V _{CC} (V)	ATEO OF	+ 25°C	T _A = -40°C to +85°C	Units	Conditions	
	xsM niM	xmlil.	Тур	Gua	ranteed Limits			
VIH.	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	stion Palay Output	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
VIL	Maximum Low Level Input Voltage	3.0	1.5	0.8	8.0 ± 0.8	etion/Delay Output	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{OH}	Minimum High Level	8.3.0	2.99	2.9	7.5 2.9	Enat V : Time	$I_{OUT} = -50 \mu\text{A}$	
	Output Voltage	70,6	0.0	0.1	8.0 ± 8.8	.,	*VIN = VII or VIH	
50	1.0 16.0	3.0	0.0	2.58	2.48	Enable Time	$I_{OH} = -12 \text{mA}$	
VOL	Maximum Low Level	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
an	Output Voltage	0.3.0	2.5	0.36	80± 0.44	V V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
I _{IN}	Maximum Input Leakage Current	3.6	7.5	±0.1	8.0± £9.0	μА	$V_{I} = V_{CC}$, GND	
loz	Maximum TRI-STATE	1.5	0.1		8.0 ± 8.8	Output	V_{I} (OE) = V_{IL} , V_{IH}	
nodzoffoeco	Leakage Current	3.6	ne we outsty	±0.25	±2.5	μΑ	$V_I = V_{CC}$, GND	
	meter quaranteed by design,	(tosis) Par	HOW IS HIGH	NO (masson) WOU	me direction, either HIGH to	toning in the sa	$V_0 = V_{CC}$, GND	

AC Electrical Characteristics: See Section 2 for Test Methodology

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued) partiaged (teroph spirited murnixed studeed A

		an	74L1	/Q125	74LVQ125	b bellio	if Military/Aerospace spe please contact the Nat	
Symbol	Parameter	V _{CC} (V)	T _A ⇒ +25°C		T _A = -40°C to +85°C	Units	Conditions Only	
		(1)	Тур	Gu	aranteed Limits		DC Input Diode Current (lad	
IOLD	†Minimum Dynamic	3.6	rating Terr	200	Am 09 - 36	mA	V _{OLD} = 0.8V Min (Note 1)	
IOHD	Output Current	3.6	- DVJ	7	va.0 + -25 va.0-	mA	V _{OHD} = 2.0V Min (Note 1)	
Icc	Maximum Quiescent Supply Current	3.6	uch inum 8.0 mont _N	4.0	40.0 Am 020 mA	μΑ Θιά	VIN TVCC ID JudiuO OD or GND VA.0- = 0V	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.6	1.0	+ 20 mA 0.5V to to V _{GC} + 0.5V	_ v	(Notes 2 and 3) OV	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.6	-1.0	Am 03 ±	٧	(Notes 2 and 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	±200 mA	٧	(Notes 2 and 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8	± 100 mA	٧	(Notes 2 and 4) flots 2 and 3	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

		745.70125	20400	74LVQ125		74LVQ125	
Symbol	Parameter	V _{CC}	+ 26°C	C _L = +25°C	C 00V (V)	T _A = -40°C to +85°C C _L = 50 pF	Units
		anteed Limits	Min	Тур	Max	Min Max	
t _{PLH} V1.0	Propagation Delay Data to Output	2.7 3.3 ±0.3	1.0 1.0	7.8 6.5	12.7 9.0	1.0 00 10 10.0	ns
t _{PHL} V1.0 = V1.0 -	Propagation Delay Data to Output	2.7 3.3 ±0.3	1.0 1.0	7.8 6.5	12.7 9.0	0.01 Voltage 0.1	ns
tpZH 03-	Output Enable Time	8.5 2.7 3.3 ±0.3	1.0	7.2 6.0	14.8 10.5	1.0 psilov ju 11.0	ns
tpzLm St -	Output Enable Time	2.7 3.3 ±0.3	1.0 1.0	9.0 7.5	14.0 10.0	1.0 16.0 1.0 11.0	ns
tPHZ IO IIV	V V	2.7 3.3 ±0.3	1.0	9.0 7.5	14.0 10.0	1.0 1.0 15.0 1.0 10.5	ns
t _{PLZ}	Output Disable Time	2.7 3.3 ±0.3	1.0	9.0 7.5	14.8 10.5	1.0 16.5 1.0 11.5	ns
toshl, toslh	Output to Output Skew* Data to Output	2.7 3.3 ±0.3	7	1.0 1.0	1.5 1.5	1.5 1.5 3TATS-IRT mum TRI-STATE	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance **Symbol Parameter** Тур Units Conditions V_{CC} = Open CIN Input Capacitance 4.5 pF

pF

1-of-8 Decoder/Demultiplexer

74LVQ138 Low Voltage

Note 1: CpD is measured at 10 MHz.

CPD

(Note 1)

General Description

The LVQ138 is a high-spend 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory onip select address decoding. The multiple input enables

 $V_{CC} = 3.3V$

Features

34

m ideal for low power/low noise 3.3V applications

Power Dissipation

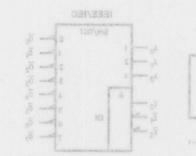
Capacitance

- # Improved latch-up immunity
- m Guaranteed incident wave switching into 750.
 - 88 4 kV minimum ESD immunity
 - # Multiple input enable for each expansion
 - M Active LOW mutually exclusive outputs
- MIL-STD-888 54AC products are available for Military/

Ordering Code: See Section 11

Logic Symbols

Connection Diagram





Description	Pin Names
Address inputs	Ao-Ae
Enable inputs	E1-E2
Enable input	E8
Outputs	Oo-O7

SOIC EIAJ	SOIC JEDEC	
74LVQ138SJ 74LVQ138SJX	74LVQ138SC 74LVQ136SCX	Order Number
M16D	M16A	See NS Package Number



pacitance

74LVQ138

Low Voltage 1-of-8 Decoder/Demultiplexer

Vcc = 3.3V

General Description

The LVQ138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVQ138 devices or a 1-of-32 decoder using four LVQ138 devices and one inverter.

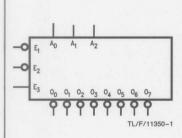
Features

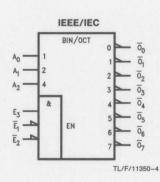
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Demultiplexing capability
- Multiple input enable for each expansion
- Active LOW mutually exclusive outputs
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

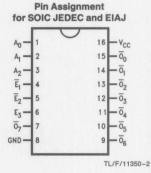
Ordering Code: See Section 11

Logic Symbols

Connection Diagram







Pin Names	Description
A ₀ -A ₂	Address Inputs
$\overline{E}_1 - \overline{E}_2$	Enable Inputs
E ₃	Enable Input
$\overline{O}_0 - \overline{O}_7$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ138SC 74LVQ138SCX	74LVQ138SJ 74LVQ138SJX
See NS Package Number	M16A	M16D

Functional Description

The LVQ138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A₀, A₁, A₂) and, when enabled, provides eight mutually exclusive active-LOW outputs $(\overline{O}_0-\overline{O}_7)$. The LVQ138 features three Enable inputs, two active-LOW $(\overline{E}_1,\overline{E}_2)$ and one active-HIGH (E_3) . All outputs will be HIGH unless \overline{E}_1 and \overline{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel ex-

pansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LVQ138 devices and one inverter (see Figure 1). The LVQ138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

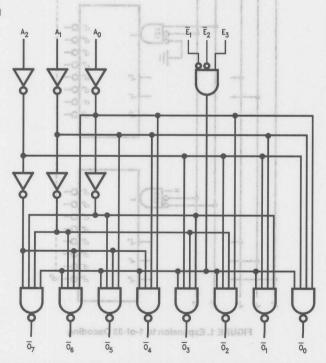
		Inp	uts		2 maril	5	3	ALI DATE AND ADDRESS	Outputs				
Ē ₁	E ₂	E ₃	A ₀	A ₁	A ₂	Ō ₀	Ō ₁	Ō ₂	Ō ₃	O ₄	O ₅	Ō ₆	07
Н	X	X	X	X	X	H	н	Н	Н	Н	н	Н	Н
X	Н	X	X	X	X	Н	Н	Н	Н	Н	H	Н	Н
X	Х	L	Х	X	X	Н	Н	Н	Н	Н	н	Н	Н
L	L	Н	L	L	L	L	Н	H	Н	н	н	Н	Н
L	L	Н	Н	L	L	H	L	H	H	Н	H	Н	Н
L	L	Н	L	Н	L	Н	Н	E	H	Н	Н	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	-L	Н	Н	Н	Н
L	L	н	L	L	н	Н	H 13	Н	Н	L	H	н	Н
L	L	Н	Н	L	н	Н	Hs	Н	Н	Н	-0-6	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	н	L	Н
L	L	Н	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	L

H = HIGH Voltage Level

L = LOW Voltage Level

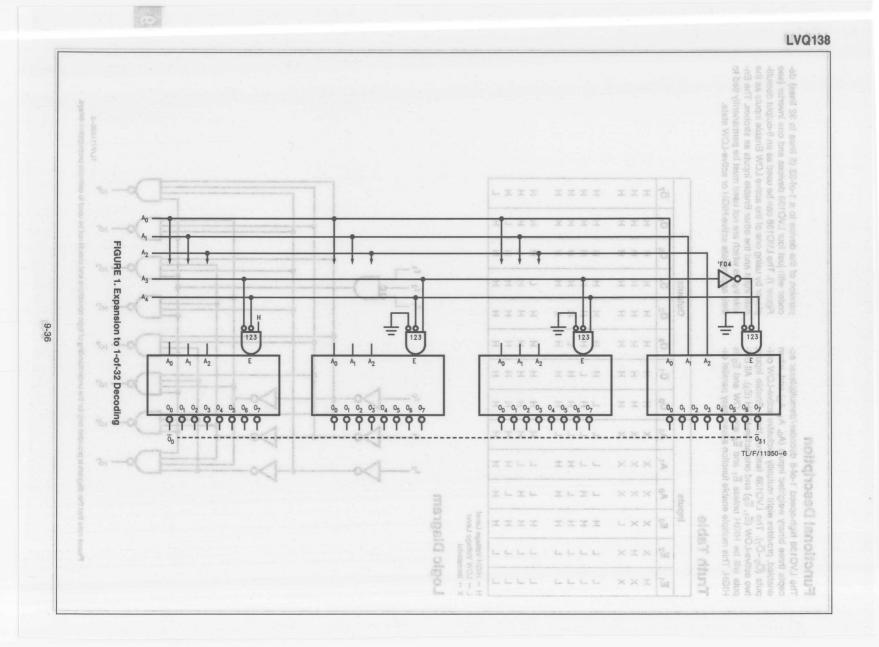
X = Immaterial

Logic Diagram



TL/F/11350-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Supply Voltage (V _{CC}) DC Input Diode Current (I _{IK})	= 0.5V to +	7.0V	4000000	oltage (V _I) Voltage (V _C	Perameter	2.0V to 3.6V 0V to V _{CC} 0V to V _{CC}
$V_{I} = -0.5V$ $V_{I} = V_{CC} + 0.5V$	0.03 + 20	0 mA 0 mA		ng Temper		lool
DC Input Voltage (V _I) DC Output Diode Current (I _{OK}) V _O = -0.5V	-0.5V to V _{CC} +	0.5V 3.0 0 mA	V _{IN} fr	m Input Edgrom 0.8V to	ge Rate (ΔV/Δt) 2.0V	125 mV/ns
$V_O = V_{CC} + 0.5V$ DC Output Voltage (V _O)		0 mA	ACC (8.8	Quiet Cutput Minimum Dynamic VOL	V.JOV
DC Output Source or Sink Current (I _O)	±50	0 mA	1.7	8.8	Maximum High Level Dynamic Input Voltage	аніл
DC V _{CC} or Ground Current (I _{CC} or I _{GND})	±200	0 mA		8.8	Maximum Low Level Dynamic Input Voltage	
Storage Temperature (TSTG) DC Latch-Up Source or Sink Current		0 mA	wol as asonal		duration 2.0 ms, one output loaded t veve switching on transmission lin	

Note: The "Absolute Maximum Ratings" are those values, we car vo nevels are closed about the besides about to reduce a solid account. beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Characteristics

	Ct = 50 pF		74LVQ138		74LVQ138		
Symbol	Parameter	V _{CC}	TA =	+25°C	T _A = -40°C to +85°C	Units	Conditions
en .	1.6 16.0	19.0	Тур	∂ Gua	ranteed Limits		An to On
VIH	Minimum High Level Input Voltage	3.0	1.5	2.0	8.01 2.0	Delay	V _{OUT} = 0.1V or V _{CC} - 0.1V
VILI	Maximum Low Level Input Voltage	3.0	1.5	0.8	8.0 ± 0.8	Delay V	V _{OUT} = 0.1V or V _{CC} - 0.1V
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$
an	Output Voltage	8.3.0	13.2	2.58	2.48	VoO	$*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
V _{OL}	Maximum Low Level	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
an	Outut Voltage	3.0	8.5	0.36	0.44	V.	$*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6	1.0 lay for any lay	±0.1	\$.0 ± 8.5 ± 1.0	μΑ	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic	3.6	HOH of Wi	M (Gest) or U.	36 and	mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}	Output Current	3.6			-25	mA	V _{OHD} = 2.0V Min (Note 1)

*All outputs loaded; thresholds on input associated with output under test. Vcc = Open

DC Characteristics (Continued) MMOOSA (COM) Sprits A murrixs M stuload A

		V _{CC}	74LV	Q138	74LVQ138	ospace sp	Conditions	
Symbol O.S	Parameter		= AT.VC	+ 25°C	T _A = -40°C to +85°C	Units		
noV of VO			Тур	Gua	ranteed Limits	Current (In		
Icc 0°88+ of 0°	Maximum Quiescent	3.6	Operatin 74LVC	Am 09-	40.0	μAV3.	V _{IN} = V _{CC} or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	Minkmum Viju fra	0.8	(NO	e (vj) e Cu X ent ((Notes 2 & 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	204	-0.8 + 0.6V	nV of V2,0—	0.5V _V	+ (Notes 2 & 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0 03±		V 90	(Notes 2 & 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8008		and Current V	(Notes 2 & 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ. Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVQ138	орегатоп.	74LV	O OG Units	
Symbol	Parameter	V _{CC}		A = +25° CL = 50 pl		T _A = to + C _L =		
	inda cons	= AT	Min	Тур	Max	Min	Max	Loughaman
t _{PLH}	Propagation Delay A _n to O _n	2.7 3.3 ±0.3	1.5	10.2 8.5	18.3 13.0	1.5 1.5	21.0 15.0	ns
t _{PHL}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	9.6 8.0	17.6 12.5	eva 1.5 _{00H}	20.0	ns
t _{PLH}	Propagation Delay E ₁ or E ₂ to O _n	2.7 3.3 ±0.3	1.5 1.5	13.2 11.0	21.0 15.0	1.5 1.5	23.0 16.0	ns
tphl Au	Propagation Delay E ₁ or E ₂ to O _n	2.7 3.3 ±0.3	1.5 1.5	11.4 9.5	19.0 13.5	1.5 1.5	21.0 15.0	ns
t _{PLH}	Propagation Delay E ₃ to O _n	8 2.7 3.3 ±0.3	1.5	13.2 11.0	21.8 15.5	1.5 1.5	23.5 16.5	ns
t _{PHL}	Propagation Delay	2.7 3.3 ±0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 1.5	20.0	ns
toshl,	Output to Output Skew* Data to Output	2.7 3.3 ±0.3		1.0	1.5 1.5	n Input	1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance V

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.

74LVQ151 active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless contract inputs. The logic function provided at the output Multiplexer output at the contract of the logic function provided at the contract of the logic function of the logic

General Description

The LVQ151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The LVQ151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

Z = E = 10 = 50 = 5, = 50 + 1, = 50 = 5, = 50 +

The LVO151 is a logic implementation of a single pole, 8position switch with the switch position controlled by the state of three Select inputs, So, S1, S2. Both true and com-

- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Pin Names 10-17

S0-S2

Ē

Z

Z

TUFFILE

Logic Symbols

IEEE/IEC 10 11 12 13 14 15 16 17 TL/F/11351-1

Description

Inverted Data Output

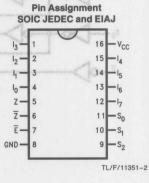
Data Inputs

Select Inputs

Enable Input

Data Output

Connection Diagram



TL/F/11351-4

Truth Table

	Inputs			Outp	uts
Ē	S ₂	S ₁	S ₀	Z	Z
Н	X	X	X	Н	L
L	L	L	L	Īo	lo
L	L	L	Н	Ī	11
L	L	Н	L	Ī ₂	12
L	L	Н	Н	Ī ₃	13
e undgrster	ed anH for the	ram isprovid	that this day	ion T ₄	14
L	Н	L	Н	Ī ₅	15
L	Н	Н	L	Ī ₆	16
L	Н	Н	Н	Ī ₇	17

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ151SC	74LVQ151SJ
	74LVQ151SCX	74LVQ151SJX
See NS Package Number	M16A	M16D

Functional Description

The LVQ151 is a logic implementation of a single pole, 8position switch with the switch position controlled by the state of three Select inputs, So, S1, S2. Both true and complementary outputs are provided. The Enable input (E) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

The LVQ151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the LVQ151 can provide any logic function of four variables and its complement.

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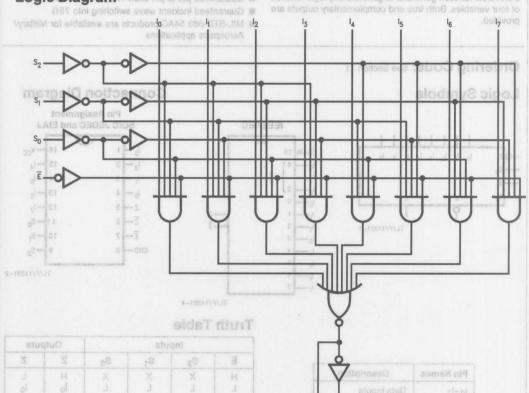
TL/F/11351-5

 $Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet S_3 \bullet \overline{S}_3 \bullet \overline{S}$ $\begin{array}{c} I_2 \circ \overline{S}_0 \circ S_1 \circ \overline{S}_2 + I_3 \circ S_0 \circ S_1 \circ \overline{S}_2 + \\ I_4 \circ \overline{S}_0 \circ \overline{S}_1 \circ S_2 + I_5 \circ S_0 \circ \overline{S}_1 \circ \overline{S}_2 + \\ I_6 \circ \overline{S}_0 \circ S_1 \circ S_2 + I_7 \circ S_0 \circ S_1 \circ \overline{S}_2 \end{array}$ @ Guarante

dynamic threshold performance Logic Diagram A wests nig-of-nig been as and a

General Description The LVQ151 is a high-speed 8-input digital multiplexer. It

data from up to eight sources. The LVO151 can be used as



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MIGA

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. -0.5V to +7.0VSupply Voltage (V_{CC}) DC Input Diode Current (I_{IK}) $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (V_I) -0.5V to $V_{CC} + 0.5V$ DC Output Diode Current (IOK) $V_0 = -0.5V$ -20 mA $V_O = V_{CC} + 0.5V$ +20 mA -0.5V to $V_{CC} + 0.5V$ DC Output Voltage (Vo) DC Output Source or Sink Current (IO) ±50 mA DC V_{CC} or Ground Current ±200 mA (ICC or IGND) Storage Temperature (TSTG) -65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating and OC Conditions

Supply Voltage (V_{CC})

LVQ 2.0V to 3.6V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)

V_{CC} @ 3.0V 3.6 thouseand mumikeM 125 mV/ns.
Supply Current
Quest Output

DC Characteristics

DC Latch-Up Source or Sink Current

	dology	74LV	Q151 0100	74LVQ151	I Chara	AU EISCITICS	
Parameter	V _{CC} (V)	IA - T29 C		T _A = -40°C to +85°C	Units	Conditions	
	3	Тур	Gua	aranteed Limits	netermenes	Symbol	
Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
Maximum Low Level Input Voltage	3.0	3.1.5	0.8	8.0) ± 0.3	ation Delay or ZV	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
Minimum High Level	3.0	2.99	2.9	2.9	SHOOT VIOLES	$I_{OUT} = -50 \mu\text{A}$	
Output Voltage	0.88.0	3.9 0.8	2.58	2.48	ation V elay	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$	
Maximum Low Level	3.0	0.002	0.1	7.5 0.1	valeo Vnoite	$I_{OUT} = 50 \mu\text{A}$	
Output Voltage	3.0	8.5	0.36	0.44	or Z v	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
Maximum Input Leakage Current	3.6	9,5	±0.1	8.0 ± 8.8 ± 1.0	μΑ	$V_{I} = V_{CC}$, GND	
	Minimum High Level Input Voltage Maximum Low Level Input Voltage Minimum High Level Output Voltage Maximum Low Level Output Voltage	Minimum High Level Input Voltage Maximum Low Level Input Voltage Minimum High Level 3.0 Minimum High Level 3.0 Output Voltage Maximum Low Level 3.0 Maximum Low Level 3.0 Maximum Low Level 3.0 Maximum Input 3.6	Parameter Vcc (V) T _A =	Parameter V _{CC} (V) T _A = +25°C Typ Gua	Parameter Vcc	Parameter VCC	

±100 mA

*All outputs loaded; thresholds on input associated with output under test.

9

DC Characteristics (Continued) TIMOSOFI (6104) Egnilla Finumban Stuloed A

		suo	74LV	Q151	74LVQ151	specified	if Military/Aerospace clesse contact the
Symbol	S Parameter	V _{CC} (V)		T _A = -40°C to +85°C	Units	Conditions	
OV to Voc		(oV) ap	Тур	Gua	ranteed Limits	(SHI)	DC Input Diode Current
OLD O'88 + o'	†Minimum Dynamic Output Current	3.6	Coerating Tr 74LVQ	An	36 0 + 20 05 V 2 0 -	mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}	Rate (AV/At)	3.6	gal muminiy LmanV		-25	mA	V _{OHD} = 2.0V (Note 1)
Icc\Vm 891	Maximum Quiescent Supply Current	3.6	V _{CC} © 3.0		00 + 40.0	μΑ	$V_{IN} = V_{CC}$ or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8	10.4 0.0 40.0-	V	(Notes 2 & 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8 _{An}	(60S.E	v ine	(Notes 2 & 3) 30 V 00 (Qual 19 00)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	-65°C to +150	v ^{(ara}	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8	yen selve "splits" The cases solve	exim V m F	(Notes 2 & 4)

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

			= AT		74LVQ151	Vec	74LVQ	151	
Symbol		Parameter	Vcc (V)	isué)	T _A = +25° C _L = 50 pl		T _A = -40°C to +85°C C _L = 50 pF		Units
VI.0	Vour P	V	2.0	Min	Тур	Max	Min	Max	HIV
t _{PLH} _{Vt.0} =		gation Delay Z or Z	2.7 3.3 ±0.3	3.0 3.0	13.8 11.5	25.3 18.0	3.0	28.0 20.0	ns
tPHL 03	The same areas.	gation Delay Z or Z	2.7 3.3 ±0.3	2.5 2.5	14.4 12.0	25.3 18.0	2.5 2.5	28.0	ns
tpLH	Propa E to Z	gation Delay or Z	2.7 3.3 ±0.3	2.5 2.5	9.6 8.0	0.18.3 13.0	2.0 2.0	20.0 14.0	ns
tphL at Val	Propa E to Z	gation Delay or Z	2.7 3.3 ±0.3	1.5 1.5	10.2 8.5	18.3 13.0	1.5 love 1.5.1 mum 1.5 lov to	20.0 14.0	ns
t _{PLH} Am SI	Propa In to Z	gation Delay or Z	2.7 3.3 ±0.3	2.5 2.5	11.4 9.5	19.7 14.0	2.0	22.0 15.5	ns
t _{PHL}	Propa In to Z	gation Delay or Z	2.7 3.3 ±0.3	2.5 2.5	11.4 9.5	21.1 15.0	2.0	23.0	ns
toshl,		t to Output Ske	ew* 2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.



74LV0157 Low Voltage Quad 2-Input Multiplexer

C	apacitanc	е			lon
	Symbol	Parameter	Тур	Units	Conditions
	CIN	Input Capacitance	4.5	pF	V _{CC} = Open
	C _{PD} (Note 1)	Power Dissipation Capacitance	45	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.

General Description

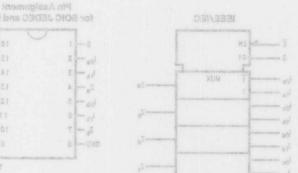
bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present

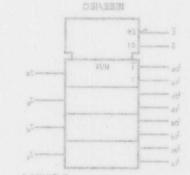
Features

- et Ideal for Iow power/Iow noise 3.3V applications
- @ Guaranteed simultaneous switching noise level and dynamic threshold performance
 - m Guaranteed pin-to-pin skew AC performance
 - m Guaranteed incident wave switching into 750.
- m MIL-STO-983 54AC products are available for Military/

Logic Symbols

Connection Diagram





Description	Pin Names
Scurce 0 Data Inputs Source 1 Data Inputs Enable Input Select Input	los-lod las-lad E
Outputs	24-24

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ157SCX 74LVQ157SCX	74LVQ157SJ 74LVQ157SJX
See NS Package Number	M16A	M16D

Input Capacitanos

t to Cpg is measured at 10 MHz.

Low Voltage Quad 2-Input Multiplexer

General Description

The LVQ157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The LVQ157 can also be used as a function generator.

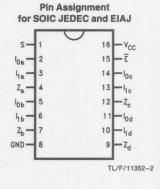
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75 Ω .
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Ordering Code: See Section 11

Logic Symbols

Connection Diagram



Pin Names	Description
l _{0a} -l _{0d}	Source 0 Data Inputs
I _{1a} -I _{1d}	Source 1 Data Inputs
Ē	Enable Input
S	Select Input
$Z_a - Z_d$	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ157SC 74LVQ157SCX	74LVQ157SJ 74LVQ157SJX
See NS Package Number	M16A	M16D

of data from two sources under the control of a common Select input (S). The Enable input (Ē) is active-LOW. When Ē is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The LVQ157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

elow:
$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
 else a speak appearing muminimal volume \overline{E}

$$Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_{c} = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the LVQ157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

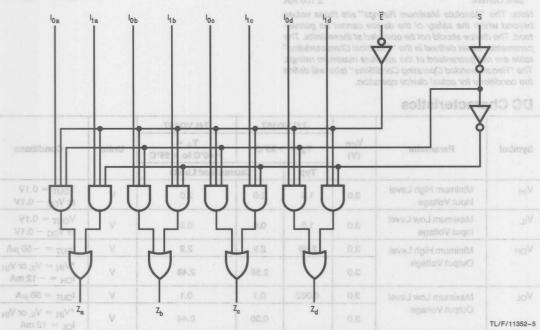
Truth Table

+20 m/	Inp	Val	Outputs	
E oc	S	I ₀	I ₁ (V)	OC Input Voltage
H.	X	X	X	Va.0-L= 6V
Am (L)+	н	X	L va.o	+ 00VL= 0V
vanL.	V or Ha o-	X	Hyper	attoy nHauo oo
L 00	L	L	X	we when no
Ann object	L	Н	X	or Still Curren

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})		-0.5	V to +7.0V
DC Input Diode Current (I_{IK}) $V_I = -0.5V$		elds'	-20 mA
$V_I = V_{CC} + 0.5V$	8	input	+ 20 mA
DC Input Voltage (V _I)	n1	-0.5V to	V _{CC} + 0.5V
DC Output Diode Current (I_{OK} $V_O = -0.5V$) X	X	-20 mA
$V_{O} = V_{CC} + 0.5V$		H	+ 20 mA
DC Output Voltage (Vo)	X	-0.5V to	VCC + 0.5V
DC Output Source	4	1 3	
or Sink Current (I _O)	11		±50 mA
DC V _{CC} or Ground Current (I _{CC} or I _{GND})			± 200 mA
Storage Temperature (T _{STG})		-65°C	to + 150°C
DC Latch-Up Source or Sink Current			± 100 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating

Supply Voltage (V _{CC})	Select input (S). The Enable input V3.6 of V0.2 il of the outputs (Z) as
Input Voltage (V _I) of end	20V of VO r inputs. The LVC157 is
Output Voltage (Vo)	OV of Vole, 2-position switch w
Operating Temperature (74LVQ	TA) 1 of the vice
Minimum Input Edge Rate VIN from 0.8V to 2.0V	$Z_{n} = \mathbb{E} * (h_{n} \circ S + h_{n} \circ S) = \mathbb{E}$ $(2 \circ h_{n} \circ S) + (2 \circ h_{n} \circ S) = (2 \circ h_{n} \circ S)$
V _{CC} @ 3.0V	125 mV/ns

 $Z_d = E * (I_1d * S + I_0d * S)$ A common use of the LVO157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is

 $Z_c = E \circ (I_{1c} \circ S + I_{0c} \circ S)$

Logic Diagram

DC Characteristics

	ŏ L		74LV	Q157	74LVQ157	-	- manual land
Symbol Parameter	Parameter	V _{CC} (V)	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Conditions
	The second second second second	1	Тур	Gua	ranteed Limits		
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	٧ ,	$I_{OUT} = -50 \mu\text{A}$
	Output Voltage	3.0	V	2.58	2.48	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
71/F/11352-5	Output Voltage	3.0	28	0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6	ina enollerego	±0.1	± 1.0	µА	$V_I = V_{CC}$, GND

^{*}All outputs loaded; thresholds on input associated with output under test.

Capacitance

DC Characteristics (Continued)

	nditions	00	74LV	Q157	74LVQ157	etemsis		Symbol
Symbol Parameter Ve.8 =	Parameter Vcc (V)		$T_A = +25^{\circ}C$ $T_A = -40^{\circ}$ to $+85^{\circ}C$		Units		Conditions	
		Тур	Guara	anteed Limits	ecitance		(Note 1)	
lold	†Minimum Dynamic Output Current	3.6			36	mA	V _{OLI} (Not	e 1)
IOHD		3.6			-25	mA	V _{OHD} = 2.0V Min (Not	
Icc	Maximum Quiescent Supply Current	3.6		4.0	40.0	μΑ	V _{IN} = V _{CC} or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.7	0.8		٧	(Notes 2 & 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	-0.8		٧	(Not	es 2 & 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		٧	(Not	es 2 & 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Not	es 2 & 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75 \(\Omega\$ for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol				74LVQ157	74LV	Q157		
	Parameter	V _{CC} (V)		T _A = +25°(C _L = 50 pF		T _A = to + C _L =	Units	
			Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay S to Z _n	2.7 3.3 ±0.3	1.5 1.5	84 7.0	16.2 11.5	1.5 1.5	19.0 13.0	ns
t _{PHL}	Propagation Delay S to Z _n	2.7 3.3 ±0.3	1.5 1.5	7.8 6.5	15.5 11.0	1.5 1.5	17.0 12.0	ns
t _{PLH}	Propagation Delay E to Z _n	2.7 3.3 ±0.3	1.5 1.5	8.4 7.0	16.2 11.5	1.5 1.5	19.0 13.0	ns
t _{PHL}	Propagation Delay E to Z _n	2.7 3.3 ±0.3	1.5 1.5	7.8 6.5	15.5 11.0	1.5 1.5	17.0 12.0	ns
t _{PLH}	Propagation Delay I _n to Z _n	2.7 3.3 ±0.3	1.5 1.5	6.0 5.0	12.0 8.5	1.0 1.0	13.0 9.0	ns
t _{PHL}	Propagation Delay I _n to Z _n	2.7 3.3 ±0.3	1.5 1.5	6.0 5.0	11.3 8.0	1.0 1.0	13.0 9.0	ns
toshl,	Output to Output Skew* Data to Output	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshL) or LOW to HIGH (tosLH). Parameter guaranteed by design.

DC Characteristics (Continued)

Capacitance

Symbol C _{IN} Inp		rameter	T 74LV Q157	yp Tar	Units	Co	onditions	
		out Capacitance 4.5		1.5	pF	oo'Vo	C = Open	Symbol
C _{PD} (Note 1)		Power Dissipation 34.0 Capacitance		State of the state	pF qyT		C = 3.3V	ionin (c
Note 1: C _{PD} is measured a	t 10 MHz.	Am	36			3.6	†Minimum Dynamic Output Current	
D = 2.0V Min (Note 1)	HOV	Am	-25			3.6		
= Vcc ND	VIIV	Au	40.0	4.0		8.6	Maximum Quiescent Supply Current	001
as 2 & 3)	(Not	٧		8.0	0.7	3.3	Qulet Output Maximum Dynamic Vot	4JOV
es 2 & 3)	IoVI)	٧		8.0-	-0.4	8.8	Quiet Output Minimum Dynamic Vot.	Votv
es 2 & 4)	(Not	ν		2.0	1.7	8.8	Maximum High Level Dynamic input Voltage	σнι∨
.es 2 & 4)	(Not	V		8.0	1.6	3.3	Maximum Low Lavel Dynamic Input Voltage	GJIV

¹Maximum test direction 2.0 ms, one output loaded at a time.

AC Electrical Characteristics: See Section 2 for Test Methodology

	0157	74LV		74LVQ157				
$T_{A} = -40^{\circ}C$ to $+85^{\circ}C$ Units $C_{L} = 50 \ pF$		$T_{\rm A} = +25^{\circ}{\rm C}$ $C_{\rm L} = 50~{\rm pF}$		Vcc (V)	Parameter	Symbol		
	xeM	allii	Max	qyT	niès			
	19.0	1.5	16.2	84 7.0	1.5	2.7 3.3 ± 0.3	Propagation Delay S to Z _n	HIG
en	17.0	1.5	15.5 11.0	7.8 6.5	1.5	2.7 3.3 ±0,3	Propagation Delay S to Z _n	
en	19.0	1.5	16.2	8.4	1.5	2.7 3.3 ± 0.3	Propagation Delay E to Z _n	HJI9
an	17.0 12.0	1.5 1.6	15.5 11.0	7.8	1.5	2.7 3.3 ± 0.3	Propagation Delay E to Z _n	
	13.0 9.0	1.0 0.1	12.0	6.0	1.5	2.7 3.3 ±0.3	Propagation Delay	PLH
вп	13.0 9.0	1.0	11.3 8.0	6.0	1.5 1.5	2.7 3.3 ± 0.3	Propagation Delay	РНС
an	1.5		1.5	1,0		2.7 3.3 ± 0.3	Output to Output Sleaw* Date to Output	OSHL

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same direction, either HIGH to LOW (LOSHL) or LOW to HIGH (togy). Persmoter guaranteed by design.



Note it incident wave switching on transmission lines with impedances as low as 750; for commercial temperature range is guaranteed for 74LVC.

Note 2: Worst case packs

Note 3: Max number of outputs defined as (n). Oata inputs are driven 6V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching, (n-1) inputs switching DV to 3.3V, Input-under-sett switching; 3.3V to threshold $(V_{\rm H,D})$, DV to threshold $(V_{\rm H,D})$, t=1 MHz.



74LVQ174 WOLA notificati (10) stock Hollit-of-WOL eth grinwollot Low Voltage Hex D Flip-Flop with Master Reset to the properties of the p

General Description

The LVQ174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

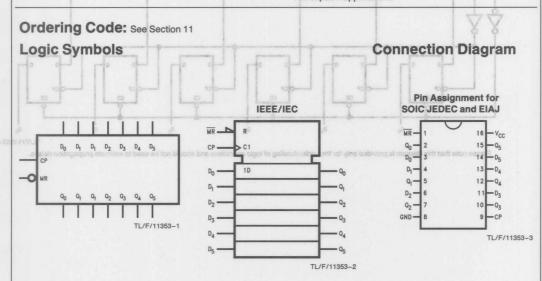
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

The LVQ174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MiR) are common to all flip-flops. Each D input's

- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω
- MIL-STD-883 54AC products are available for Military/ Aerospace applications

Functional Description

the Clock and Master Reset are commo



Pin Names	Description
D ₀ -D ₅	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q ₀ -Q ₅	Outputs

	SOIC JEDEC	SOIC EIAJ
Order Number	74LVQ174SC	
	74LVQ174SCX	74LVQ174SJX
See NS Package Number	M16A	M16D

Functional Description

The LVQ174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The LVQ174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

to least for low power/low noise 3.3V applica & Gueranteed simultaneous switching noise level and

Truth Table

	Inputs					
MR	СР	D	Q			
L	X	X	AF BALS			
Н	_	H	H			
FIHO-F	1	ingtio)	/ weck!			
Н	L	X	Q			

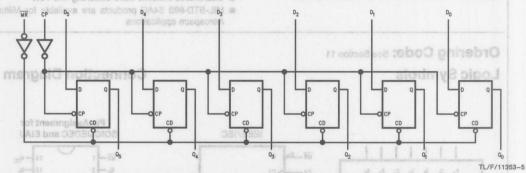
during the LOW-to-HIGH clock transition. The device has a

H = HIGH Voltage Level

L = LOW Voltage Level

= LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Input Diode Current (I _{IK})		LVQ Input Voltage (VI)			2.0V to 3.6V 0V to V _{CC}		
$V_1 = -0.5V$	= 20 mA		ige (V _O)		OV to V _{CC}		
VI = VCC + 0.5V	+20 mA -0.5V to V _{CC} + 0.5V		Operating Temperature (T _A) many muminity 74LVQ				
O (Complete)	-20 mA +20 mA	V _{IN} from 0 V _{CC} @ 3.0	0.8V to 2.0	Rate (ΔV/Δt) DV	125 mV/ns		
DC Output Voltage (V _O) -0.5V to V _{CC}	+ 0.5V		3.6	Maximum Quiescent Supply Current	001		
	±50 mA	7.0	3.3	Quiet Output Maximum Dynamic V _{OL}	Anon		
(I _{CC} or I _{GND}) ± Storage Temperature (T _{STG}) −65°C to	± 200 mA + 150°C	8.0-	3.3	Quiet Output Minimum Dynamic Vol			
	± 100 mA	1.8	8.8	Maximum High Level Dynamic Input Voltage			
Note: The "Absolute Maximum Ratings" are thos beyond which the safety of the device cannot be teed. The device should not be operated at these line parametric values defined in the "Electrical Charac."	guaran- mits. The	1.6	8.8	Maximum Low Level Oynamic Input Voltage	VILD		

DC Characteristics of VE.E. griddlive teet-inbrut-lugni. VE.E of VD griddlive etuqui (1 - n). griddlive (n) studyi at 00 to redmun xsM := stoM

	Parameter			A = +25 G		S1840 Units	SolutionS OA	
	TA = -40°C		Typ Guar		ranteed Limits			
ViH	Minimum High Level Input Voltage	3.0	791.5 = J	2.0	2.0	ratemen V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
VIL	Maximum Low Level Input Voltage	3.0	9yT 1.5	MIM 80 8.0	0.8	um Cicek	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
Voн	Minimum High Level Output Voltage	3.0	2.99	2.90.5	8.0 ± 8.8 2.9	ancy gation Dela	OUT = -50 HA	
en	1.5 12.5	3.0	10.2	2.58	2.48	ale C You's	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -12 \text{ mA}$	
VoL	Maximum Low Level Output Voltage	3.0	0.002	0.5 2.61.0	0.1	sleG Voite	= 50 uA	
en	1.5	3.0	1.0	0.36	0.44	V oil	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
N specification	Maximum Input Leakage Current	3.6	on delay for a		orit neewit± 1:0eretilb erit to		Vi = Voc GND	

^{*}All outputs loaded; thresholds on input associated with output under test.

Note 3: Max number of outputs defined as (n). Data inputs are driven 6V to 3.3V, one output at GND.

Solv of Vo	raiametei	(V)	IA = +	25°C VO.5+	Conditions Conditions		
DV to Vcc		(01/) ali	Тур	Guar	anteed Limits	(NII) toer	DC Input Diode Car
OLD + OF	†Minimum Dynamic Output Current	3.6	Operating Ti 74LVQ	Am 09 V8.0 H	36 30V of Vo.0—	mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}	Pale (AV/At) V	3.6) mon MIV 0.8 © GOV	Am os	-25	mA Am	V _{OHD} = 2.0V Min (Note 1)
lcc	Maximum Quiescent Supply Current	3.6		4.0	99 V 01 40.0	μΑ(ο\	V _{IN} = V _{CC} or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.7	0.8	±	v (e	(Notes 2, 3) 10
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.6	-0.8	6± F 41 0°58—	(p <mark>Y</mark> 2T) e	(Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.8	2.0 1 00	manufactured on theory	V	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	o device cannot be g operated at these lim		(Notes 2, 4)

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

	Control of the second of the s		F29527	And the state of t	NEW C	Egyptic State Community of the ETS	Later and mercury of \$1.50
Section 1881	-	40'0 to +85'0		74LVQ174	(50)	74LVQ174	incontri é es
Symbol	Parameter	V _{CC} (V)		C _L = +25°C C _L = 50 pF	3.0	T _A = -40°C to +85°C C _L = 50 pF	
VI 0 = moV	(1.0 = vanV		Min	Тур	Max	Min Max	nV
f _{max} 0 -	Maximum Clock Frequency	2.7 3.3 ±0.3	60 90	90 100	0.8	50-patioV tugni 70	MHz
t _{PLH}	Propagation Delay CP to Q _n	2.7 3.3 ±0.3	2.0	10.8 9.0	16.2 11.5	1.5 18.0 1.5 12.5	ns
t _{PHL} SI	Propagation Delay CP to Q _n	2.7 3.3 ±0.3	2.0	10.2 8.5	15.5 11.0	1.5 17.0 1.5 12.0	ns
t _{PHL}	Propagation Delay MR to Qn	2.7 3.3 ±0.3	2.5	10.8 9.0	16.2 11.5	2.0 18.0 2.0 12.5	ns
toshl,	Output to Output Skew*	2.7 3.3 ±0.3	0.36	1.0	1.5	1.5 1.5	ns
C 11/2 0 1 20 00 1						TOTAL PROTERNIA SALE	100

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Ordering Code Logic Symbol

Truth Tables

AC Operating	Requirements:	See Section 2 for Test Methodology
--------------	---------------	------------------------------------

			74LV	Q174	74LVQ174	5 2 2
Symbol	Parameter	V _{CC} (V)	T _A = C _L =		T _A = -40°C to +85°C C _L = 50 pF	Units
		Driver	Тур	Guaran	teed Minimum	Low A
t _s	Setup Time, HIGH or LOW D _n to CP	2.7 3.3 ±0.3	3.0 2.5	8.0 6.5	10.0 7.0	ns
th	Hold Time, HIGH or LOW D _n to CP	2.7 3.3 ±0.3	1.2 1.0	4.0 3.0	4.5 3.0	DASOINS enil
t _w	MR Pulse Width, LOW	2.7 3.3 ±0.3	1.2	7.0 10 10 10 5.5	tilmanta 10.0 leho au vilaneo 17.0 density	d brians vinb
tw	CP Pulse Width	2.7 3.3 ±0.3	1.2 1.0	7.0 5.5	10.0 7.0	ns
t _{rec}	Recovery Time MR to CP	2.7 3.3 ±0.3	0 0	3.5 2.5	3.5 2.5	ns

Capacitance eve ere aroutong COARE ESS-CTS-JIM

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	23	pF	V _{CC} = 3.3V

st 4 kV minimum ESD immunity

Note 1: CPD is measured at 10 MHz.



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	30 Q	
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	Ö	in the same
T-11811\F\IT		

Description	Pin Names
TRI-STATE Output Enable Inputs	OE ₁ , OE ₂
Inputs	lo-ky

	903C	SOIC	SSOP
Order Number	74LVG2408CX 74LVG2408CX	74LVQ240SJX 74LVQ240SJX	74LVQ248GSCX 74LVQ248SCX
See NS Packege Number	BOSM	M20D	MCAZO

Ontputs	etuqni		
(Pine 12, 14, 16, 19)	nl nl		
H			
J			
Z			

Outpute	aluqni		
(Pins 3, 5, 7, 0)	n [§]	ōĒ2	
Н			
Z	- X	and the second	

Z = High Impedance



74LVQ240 -- 01

$T_A = +25^{\circ}C$ $C_L = 58 \, pF$ Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

■ Ideal for low power/low noise 3.3V applications

Operating Requirements: See Section 2 for Test Methodology

- Implements patented Quiet Series EMI reduction
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

nput Capacitance

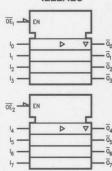
Power Dissipation

Ordering Code: See Section 11

Logic Symbol

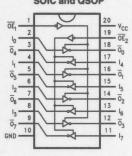
Connection Diagram

IEEE/IEC



TL/F/11611-1

Pin Assignment, SOIC and QSOP



TL/F/11611-2

Symbol

Truth Tables

Inpu	ıts	Outputs
OE ₁	In	(Pins 12, 14, 16, 18)
L	L	Н
L	Н	L
Н	X	Z

Inpu	its	Outputs	
OE ₂	In	(Pins 3, 5, 7,	
L	L	Н	
L	Н	L	
Н	X	Z	

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level Z = High Impedance

Pin Names	Description		
OE ₁ , OE ₂	TRI-STATE Output Enable Inputs		
I ₀ -I ₇	Inputs		
O ₀ -O ₇	Outputs		

	SOIC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ240SC 74LVQ240SCX	74LVQ240SJ 74LVQ240SJX	74LVQ240QSC 74LVQ240SCX
See NS Package Number	M20B	M20D	MQA20

Supply Voltage (V _{CC}) DC Input Diode Current (I _{IK})	0.5V to +7.0V	Input Volta Output Vol		1939/16/18/1	0V to V _{CC} 0V to V _{CC}
$V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage (V _I)	-20 mA +20 mA -0.5V to V _{CC} + 0.5V	74LVQ	0.6	the (T _A) manual Dynami (AT) are 140°	C to +85°C
DC Output Diode Current (I_{OK}) $V_O = -0.5V$	-20 mA	Minimum II V _{IN} 0.8V V _{CC} @ 3	to 2.0V	Rate ΔV/Δt	125 mV/ns
$V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O)	+20 mA -0.5V to V _{CC} + 0.5V		3.6	Maximum Quiescent Supply Qurrent	
DC Output Source or Sink Current (I _O) DC V _{CC} or Ground Current (I _{CC} or I _{GND})	±50 mA			Maximum TRI-STATE Leakage Current	
Storage Temperature (T _{STG}) DC Latch-Up Source or	-65°C to +150°C			Quiet Output Maximum Dynamic Vot	
Sink Current Note: The "Absolute Maximum beyond which the safety of the		-0.4		Quiet Output Minimum Dynamic Vot.	
teed. The device should not be parametric values defined in the	operated at these limits. The "Electrical Characteristics"			Maximum High Level Dynamic Input Voltage	анг ^у
table are not guaranteed at the The "Recommended Operating the conditions for actual device	Conditions" table will define	1.6	3.8	Maximum Low Level Dynamic Input Voltage	GT8 _A

DC Characteristics

Symbol	present of VO (callV) blockswift of Parameter	V _{CC} (V)	74LVQ240 T _A = +25°C		74LVQ240	(in) as bentined its (in)	to to redman xsM st ateM and to redman xsM st stsM Conditions ^M F
					T _A = -40°C to +85°	Units	
			Тур	Gua	aranteed Limits	when our model is	aniskanis na
VIH	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$
ns	2.0 15.0	0.84.0	8.4	2.58	2.48	gation Dalay	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level Output Voltage	0.83.0	0.002	0.1	7.20.1	it En V ole Time	I _{OUT} = 50 μA
811	1.0 20.0	0.83.0	10.2	0.36	0.44	t Dis V bls Time	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
IIN	Maximum Input Leakage Current	3.6	1.0	±0.1	± 1.0	tuqrµAor ti	$V_{J} = V_{CC}$, GND

^{*}All outputs loaded; thresholds on input associated with output under test.

notabilities and a set to study output associated with output under test.

notabilities and a set to study output associated with output and set to study output and set to study output and set to se

DC Characteristics (Continued) 111110000A (etc.) 201116F mumixsM stuloedA

		shoi	74LV	Q240	74LVQ240	no Nation	If Military/Aerospa please contact the
Symbol	Parameter	V _{CC} (V)	TA = +25°C		-40°C to +85°C	Units	Conditions
OV to Voc		(oV) ega	Тур	Gua	ranteed Limits	(NI) Ine	DC Input Diode Curr
Octo	†Minimum Dynamic T) 911 Output Current	3.6	Operating 74LVQ.	Am 0	36 + 20 V 01 V 3.0 -	mA	V _{OLD} = 0.8V Max (Note 1)
IOHD 80 MV/na	Rate AV/At	V3.6 of	VIII muminili V _{IIV} 0.8V	Am 0	-25	(xomAnen	V _{OHD} = 2.0V Min (Note 1)
lcc	Maximum Quiescent Supply Current	3.6		4.0/3.0	+ 00V 0/40.0) -	μΑ (6)	V _{IN} = V _{CC} or GND
loz	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA	$V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	8.0	-65°C to +1	(EVST)	(Notes 2, 3) stor8
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4		£30 Railings" are those v	Nes Vinum	(Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0	operated at these limits "Electrical Characteri.	uid ryt be c lined in the	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	abeolute maximum ra Conditions" table will c oneration.	teed at me CpcVating tual davice	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n – 1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

$V \cap \Omega = \pi$	eucy I				0,	Jesses I rigital reasonigital I	View .
V1.0 - o	or Vo	2.0		74LVQ240	0,6	74LVQ240	
Vr.0 = - Symbol 0 Au 08 - =	Parameter Parameter	8.0V _{CC} (V)	8.0	T _A = +25° C _L = 50 pl		T _A = -40°C to +85°C C _L = 50 pF	Units
	· ·	6.5	Min	Тур	Max	Min lov had Max	
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	2.7 3.3 ±0.3	2.0	8.4 7.0	14.0	2.0 15.0 2.0 10.5	ns
t _{PZL} , t _{PZH}	Output Enable Time	3.3±0.3	2.5 2.5	9.6	0.16.9 12.0	2.5 18.0 2.5 12.5	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	2.7 3.3 ±0.3	1.0	10.2 8.5	19.0 13.5	1.0 20.0 1.0 14.0	ns
toshl, oov	Output to Output Skew *Data to Output	2.7 3.3 ±0.3	1.0±	1.0 1.0	8.1.5 1.5	InomuO agesisci 1,5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

LVQ240

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	70	pF	V _{CC} = 3.3V

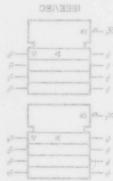
Note 1: CPD is measured at 10 MHz.

employed as a memory address driver, clock driver and bus

- # Ideal for low power/low noise 3.3V applications
- # Implements patented Quiet Series EMI reduction
- MANAGED AND AND AND AND AND COOP AND AND COOP
- Sugranteed simultaneous switching noise level and
 - a Improved latch-up immunity
 - # Guaranteed incident wave switching into 75Ω
 - at 4 kV minimum ESD immunity
- m MIL-STD-883 54ACQ products are available for Mili-

Ordering Code: See Section 11

Logic Symbol



Connection Diagram

Pin Assignment for



Outputs		eqni
(Pins 12, 14, 16, 18)	rs [§]	,30
1	1 4	1
H	H H	1

Outputs	81	uqni
(Pins 3, 5, 7, 0)	n?	OE2
		3

	= HIGH Voltage Level
Z = High Impedance	

Description	Pin Names
TRI-STATE Output Enable Inputs	ō€₁, 0€₂
Outputs	

	SOIC JEDEC	SOIC EIAJ	
Order Number			
See NS Parkage Number		M20D	



tymbol Parameter Typ Units
input Capacitance 4.6 pF
Power Dissipation

74LVQ241

Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

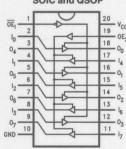
Ordering Code: See Section 11

Logic Symbol

TL/F/11355-1

Connection Diagram

Pin Assignment for SOIC and QSOP



TL/F/11355-2

Capacitance

Truth Tables

Inpu	ıts	Outputs
ŌĒ ₁	In	(Pins 12, 14, 16, 18)
L	L	L
L	Н	Н
Н	X	Z

Inputs		Outputs	
OE ₂	In	(Pins 3, 5, 7, 9)	
L	X	Z	
н н		Н	
Н	L	L	

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level Z = High Impedance

Pin Names	Description
OE ₁ , OE ₂	TRI-STATE Output Enable Inputs Inputs
00-07	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	The state of the s	The second secon	74LVQ241QSC 74LVQ241QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum	Absolute Maximum Rating (Note)		nmend	ed Operating	DC Cha
If Military/Aerospace specific please contact the Nationa Office/Distributors for available Supply Voltage (VCC)	I Semiconductor Sales	Supply Vo Input Volta Output Vo	ltage (V _{CC}) age (V _I)	Parameter	2.0V to 3.6V 0V to VCC 0V to VCC
DC Input Diode Current ($I_{ K}$) $V_{ } = -0.5V$ $V_{ } = V_{CC} + 0.5V$ DC Input Voltage ($V_{ }$)	-20 mA +20 mA -0.5V to V _{CC} + 0.5V	Operating 74LVQ	Temperatu	ire (T _A) OmanyO mumb = 40 Rate ΔV/Δt muO mgayO	-
DC Output Diode Current (I _{OK}) $V_{O} = -0.5V$	-20 mA	V _{IN} 0.89	V to 2.0V 3.0V		125 mV/ns
V _O = V _{CC} + 0.5V DC Output Voltage (V _O)	+ 20 mA -0.5V to V _{CC} + 0.5V			Maximum Quiescent Supply Current	col
DC Output Source or Sink Current (I _O) DC V _{CC} or Ground Current (I _{CC} or I _{GND})	± 50 mA 0±		3.6	Maximum TRI-STATE Leakage Current	zol
Storage Temperature (T _{STG}) DC Latch-Up Source or	-65°C to +150°C	0.4	8.8	Quiet Ourput Maximum Dynamic Vot	Volp
Sink Current Note: The "Absolute Maximum		-0.4	8.8	Quiet Output Minimum Dynamic V _{QL}	VJ0V
beyond which the safety of the teed. The device should not be o parametric values defined in the	perated at these limits. The	1.6	9.3	Maximum High Level Dynamic Input Voltage	аніV
table are not guaranteed at the The "Recommended Operating of the conditions for actual device	Conditions" table will define	1.6	8.8	Maximum Low Level Dynamic Input Voltage	O.BV

DC Characteristics no entergeneral information of the set of the s

		.gp	74L\	VQ241	74LVQ24	11 (1) 38	utputs defined	Mote at Max number of o
Symbol Parameter		V _{CC} (V) T _A = +2		+25°C	25°C T _A = -40°C to +85°C		Units	Conditions
			Тур	Gu	aranteed Limits	vatar	anoda l	AC Elastrias
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0		٧	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	+ 1.5	0.8	8.0 V _{CC}	7	Paramete	$V_{OUT} = 0.1V$ or $V_{CC} = 0.1V$
VoH	Minimum High Level	3.0	2.99	2.9	2.9		٧	$I_{OUT} = -50 \mu A$
	Output Voltage	3.0	7yp 7.8	2.58	2.48	ysl	v Degation De	$*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
Vol	Maximum Low Level	3.0	0.002	0.20.1	8.0 ± 8.8 0.1		a to Output	$I_{OUT} = 50 \mu\text{A}$
an	Output Voltage	81 3.0	9,6 0.8	8.S 8.0.36	5.5 5.0 ± 6.8	Time	put Enable	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
IN	Maximum Input Leakage Current	3.6	10.2	0.±0.1	7.S 8.0 ± 8.8 ± 1.0	Time	put Neable	V _I = V _{CC} , GND
*All outputs lo	paded; thresholds on input associ	ated with outp	out under test		2.7 3.3 ±0.3	li li	put to Outpu	200 300 40

Thisximum test duration 2.0 ms, one output loaded at a time.

Symbol	Parameter	V _{CC} (V)	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Conditions
DOV of VO	(OV) SESI	Тур	Gua	ranteed Limits	(sal) ins	DC Input Diode Cum	
IOLD + or	†Minimum Dynamic Output Current	3.6	Z4LVQ Minimum	Am Va.0	36	mA	V _{OLD} = 0.8V Max (Note 1)
OHD 351		3.6/0	V _{CC} © 3	Am	-25	610mAner	V _{OHD} = 2.0V Min (Note 1)
lcc	Maximum Quiescent Supply Current	3.6		4.0	+ 00 40.00 -	μΑ ($V_{IN} = V_{CC}$ or GND
loz	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μA memu	$V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8	r + of Orde	(TSV)	(Notes 2, 3) and 3
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	-0.8 ₋₁	±30 Ratings" are those vi	mamV _{25A}	(Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0	peraled at these limits "Electrical Characearls	e ed t V r bla geed in the	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	absolute meximum rai. Condisona" table will d convention	Grad at End	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 750 for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n – 1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

V1.0 - ac	V 10	V	0.0	2.0	74LVQ2	41 0.8	74LVQ241	
Symbol	V 10	Parameter	NO VCC (V)	8.0	T _A = +2 C _L = 50		T _A = -40°C to +85°C C _L = 50 pF	Units
= -50 µA = Vu or Vu			2.9	Min	Тур	Max	Min Wax	HOW
t _{PLH}	MITTER THE PROPERTY.	ppagation Delay ta to Output	2.7 3.3 ± 0.3	2.0	7.8	12.7	2.0 14.0	ns
tPZL V	√ Ou	tput Enable Time	2.7 3.3 ±0.3	2.5 2.5	9.6 8.0	18.3 13.0	2.5 19.0 2.5 13.5	ns
t _{PHZ} , t _{PLZ}	Ou	tput Disable Time	2.7 3.3 ±0.3	1.0	10.2 8.5	20.4 14.5	1.0 21.0 1.0 15.0	ns
toshl, toshh		tput to Output ew *Data to Output	2.7 3.3 ±0.3		1.0	1.5	nan fugrii no strioiteani 1.5 laad 1.5	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

Symbol	Parameter	Тур	Units	CONTINUE	danamak es.
CIN	Input Capacitance	4.5	pF	V _{CC} = Open	THE RESIDENCE OF THE PARTY OF T
C _{PD} (Note 1)	Power Dissipation Capacitance	70	pF	V _{CC} = 3.3V	ILVQ244

with TRI-STATE® Outputs

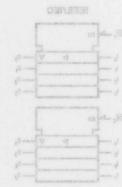
General Description

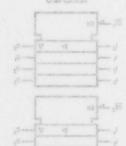
Features

- soldest for low power/low noise 3.3V applications
- m limplements patiented Oulet Series EMI reduction
- If Queranteed simultaneous switching noise level and

 - M Guaranteed incident wave switching into 750
 - # 4 kV minimum ESD immunity

Logic Symbol

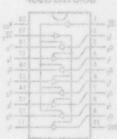




aeldsT riturT

efuqiuQ	Inputs		
(Pins 12, 14, 16, 19)	nl		
	3	1	
H			
2			

Outputs	(Inputs		
(Pins 3, 6, 7, 9)	and I		
	H		
	X		



Description	
TRI-STATE Output Enable Inputs	OE₁, OE₂
	70-00

930814068	SOICHIAL	29031 2108	
74LVQ244QSCX 74LVQ244QSCX			Order Number
MOARO	GOSM		See NS Package Plumber



pacitance

74LVQ244

Symbol asimil Parameter Typ 4.5 Input Capacitance Capacitance it Cpg is measured at 10 MHz.

Vcc = 3.3V Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

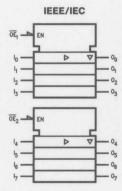
General Description

The LVQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

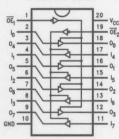
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Ordering Code: See Section 11 **Logic Symbol**



Connection Diagram

Pin Assignment for **SOIC and QSOP**



TL/F/11356-2

Truth Tables

Inpu	its	Outputs
OE ₁	In	(Pins 12, 14, 16, 18)
L	L	L
L	Н	Н
Н	X	Z

Inpu	its	Outputs
OE ₂	In	(Pins 3, 5, 7, 9)
L	L	L
L	Н	Н
Н	X	Z

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Pin Names	Description
OE ₁ , OE ₂	TRI-STATE Output Enable Inputs
10-17	Inputs
00-07	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number			74LVQ244QSC 74LVQ244QSCX
See NS Package Number	M20B	M20D	MQA20

TL/F/11356-1

Absolute Maximum Rating (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})		-0.5V to $+7.0V$
DC Input Diode Current (I _{IK})		ethni.l bashna
$V_1 = -0.5V$ $V_1 = V_{CC} + 0.5V$	Am	-20 mA +20 mA
DC Input Voltage (V _I)		-0.5 V to $V_{CC} + 0.5$ V
DC Output Diode Current (low	1	

-20 mA $V_0 = -0.5V$ $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (Vo) -0.5V to $V_{CC} + 0.5V$

DC Output Source or Sink Current (IO) ±50 mA DC V_{CC} or Ground Current (ICC or IGND) ±400 mA Storage Temperature (TSTG) -65°C to +150°C

Sink Current Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not quaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating **Conditions**

Supply Voltage (VCC) QVJ + 25°C 2.0V to 3.6V Input Voltage (VI) OV to Vcc Output Voltage (VO) OV to VCC Operating Temperature (T_A) 74LVQ -40°C to +85°C

Minimum Input Edge Rate ΔV/Δt Maximum Cules: VIN from 0.8V to 2.0V

125 mV/ns V_{CC} @ 3.0V

DC Electrical Characteristics

DC Latch-Up Source or

			74L	VQ244	74LVQ244		$(V_{BKD}), t = 1 MHz,$	
Symbol	Parameter	V _{CC} (V)	TA = +25°C		T _A = -40°C to +85°C	Units	Conditions	
	74LV0244	545	Тур	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	20 ^V 2.0	ParaVioter	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{OH}	Minimum High Level	3.0	2.99	2.9	2.9	abed Witage	$I_{OUT} = -50 \mu\text{A}$	
en	Output Voltage	3.0	a.e	2.58	2.48	ut En V ule Ti	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$	
V _{OL}	Maximum Low Level	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
	Output Voltage	3.0	0.6	0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
IN	Maximum Input Leakage Current	3.6	0.1	±0.1	0 ± 8.8 ± 1.0 Mg/	O or pA a	$V_{I} = V_{CC}$, GND	

±300 mA

^{*}All outputs loaded thresholds on input associated with output under test.

Conditions			
V _{OC} = Open	Эq		
V6.6 = 3.3V			

DC Electrical Characteristics (Continued)

Symbol		suo	74LV	Q244	74LVQ244	ciffed de onel Sei	If Williamy/Aerospace spe please contact the Nat
	Parameter	V _{CC} (V)	T _A = +25 °C		T _A = -40°C to +85°C	Units	Conditions Office (2007) egado Videus
anV of VO		(nV) eas	Тур	Guara	nteed Limits		DC Input Diode Current (IIK)
I _{OLD}	†Minimum Dynamic	3.6	perating T) Ai	105 + 36	mA	V _{OLD} = 0.8V Max (Note 1)
IOHD	Output Current	3.6	7ALVQ	. Vi	0 + 03 25 V3.0	mA	V _{OHD} = 2.0V Min (Note 1)
loc an\Vm 8\$	Maximum Quiescent Vo Supply Current	3.6	V _{IN} from	4.0 A	0.00 - 40.0	μА (VIN = VCC of higher of or GND
loz	Maximum TRI-STATE Leakage Current	3.6		±0.25	±2.5	μΑ	$V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8 A	±400 n	٧	(Notes 2,3) 10 10 00 V 00 (aug) 10 00()
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	-0.8	-85°C to +150	٧	(Notes 2, 3) The Taylor of the Country of the Count
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3	1.7	2.0	s" are those values cannot be cuses	urn Vating	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8	d at these limits. Frical Characteristic	ne operate the V Elect	(Notes 2, 4) Ob anti-book

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75 \(\Omega\$ for commercial temperature range is guaranteed for 74LVQ. Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (VILD), 0V to threshold

AC Electrical Characteristics: See Section 2 for Test Methodology

			waranteed Limite		T	74LVQ2	44		74LVQ244	
Symbol	or Vo	Parameter	V _{CC} (V)	2.0		T _A = +2 C _L = 50		la	T _A = -40°C to +85°C C _L = 50 pF	Units
V1:0 = 0	100.00	V	8.0	0.8	Min	а. Тур	0.8 Max	83	Min Max	31/
t _{PHL} ,	THO	pagation Delay ta to Output	2.7 3.3 ±0.3	200	2.0 2.0	8.4 7.0	0.E 12.7 9.0	10	2.0 14.0 2.0 9.5	ns
t _{PZL} , t _{PZH}	Out	tput Enable Time	2.7 3.3 ±0.3		2.5 2.5	9.6 8.0	16.9 12.0		2.5 18.0 2.5 12.5	ns
t _{PHZ} , t _{PLZ}	Out	tput Disable Time	2.7 3.3 ±0.3		1.0 1.0	10.8 9.0	19.0 0.8 13.5	100	1.0 20.0 1.0 14.0	ns
toshl,	2.6	tput to Output ew* Data to Output	2.7 3.3 ±0.3	0 ±		1.0 1.0	1.5 8.8 1.5		1.5 fuqni mumbasi/5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD}	Power Dissipation Capacitance	70	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.



74LVQ245

Low Voltage Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

The LVQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 12 mÅ at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

■ Ideal for low power/low noise 3.3V applications

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

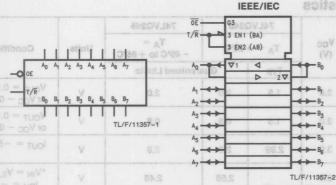
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity T outstagme Tepanote
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54 ACQ products are available for Military/Aerospace applications

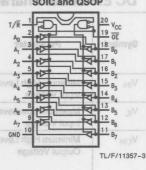
Ordering Code: See Section 11

Logic Symbols

Connection Diagram

Pin Assignment for SOIC and QSOP





Truth Table

	Pin Names	Description
V	OE OT/R	Output Enable Input Transmit/Receive Input
	A ₀ -A ₇	Side A TRI-STATE Inputs or TRI-STATE Outputs
	B ₀ -B ₇	Side B TRI-STATE Inputs or TRI-STATE Outputs

20	lnp	outs	Outputs
	ŌĒ	T/R	Outputs
	L	L	Bus B Data to Bus A
	L	e H 390	Bus A Data to Bus B
	Н	X his	HIGH-Z State

- H = HIGH Voltage Level L = LOW Voltage Level
- X = Immaterial

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ245SC 74LVQ245SCX	74LVQ245SJ 74LVQ245SJX	74LVQ245QSC 74LVQ245QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Office, Distributors for availability	ty and oppositionations.		
Supply Voltage (V _{CC}) DC Input Diode Current (I _{IK})	-0.5V to $+7.0V$	Supply Voltage (V _{CC}) LVQ	2.0V to
$V_1 = -0.5V$	-20 mA	Input Voltage (V _I)	0V to
$V_I = V_{CC} + 0.5V$	+20 mA	Output Voltage (V _O)	OV to
DC Input Voltage (V _I)	-0.5 V to $V_{CC} + 0.5$ V	Operating Temperature (T _A)	TINCH TINEN
DC Output Diode Current (IOK)		74LVQ	-40°C to +8
$V_{O} = -0.5V$ $V_{O} = V_{CC} + 0.5V$	-20 mA +20 mA	Minimum Input Edge Rate (2 V _{IN} from 0.8V to 2.0V	The LVO215 conta (tA\VA
DC Output Voltage (V _O)	$-0.5V$ to $V_{CC} + 0.5V$	V _{CC} @ 3.0V	125 mV
DC Output Source or Sink Current (I _O)	Am 05±kagas	ansmit/Receive (T/R) input deter- ate flow through the bidirectional	
	Guaranteed simultan		
Storage Temperature (T _{STG})	-65°C to +150°C	put Enable input, when HiGH, dis- ov placing them in a HIGH 2 condi-	
DC Latch-Up Source or		merce a cream a se count Account Ac	duras ocurs A circa a portas

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum raings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating **Conditions**

Supply Voltage (V _{CC})	74LVO245
LVQ	2.0V to 3.6V
Input Voltage (V _I)	0V to V _{CC}
Output Voltage (V _O)	OV to V _{CC}
Operating Temperature (T _A)	C-1111 111111
	-40°C to +85°C
Minimum Input Edge Rate (Δ\	//At) thoo RESOV Lent
V _{IN} from 0.8V to 2.0V	
V _{CC} @ 3.0V	125 mV/ ns
Transmit/Receive (T/R) Input det	the A and B ports. The

Ordering Code: See Section 11

Logic Symbols

DC Electrical Characteristics

Sink Current

y 0s 1	DY CBL W	74LVQ245		74LVQ245				
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions	
A 22 6		47	Тур	Gua	ranteed Limits	A A A A	A of 30 0-	
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V 20 10	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	٧	$I_{OUT} = -50 \mu A$	
		3.0	Secretarions ST of the car T	2.58	2.48	٧	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$	
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	nollosofipilon	V	$I_{OUT} = 50 \mu A$	
A oug o	高/Y	3.0	30	0.36	rout Enel 44.0 out	O V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = +12 \text{ mA}$	
Ing aug o	CHARLES CO. CO.	3.6	1	±0.1	NO A TRI-STATE Inputs	μΑ	$V_{I} = V_{CC}$, GND	

±300 mA

^{*}All outputs loaded; thresholds on input associated with output under test.

		SORO JEDRE	
	74LVQ245SJX 74LVQ245SJX		
MGARO			See NS Package Number

Capacitance

DC Electrical Characteristics (Continued)

	I For The I	8/	olibra4LV	/Q245@finU	74LVQ245	Paramute	Symbol	
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = 9008 -40°C to +85°C	Units Units	Conditions	
		-	Тур	Guara	anteed Limits	sianiff sour	9	
IOLD	†Minimum Dynamic Output Current	3.6	V _{CC} = 3.5	70	36	mA	V _{OLD} = 0.8V Max (Note 1)	
I _{OHD}		3.6			-25	mA	V _{OHD} = 2.0V Min (Note 1)	
loc	Maximum Quiescent Supply Current	3.6		4.0	40.0	μΑ	$V_{IN} = V_{CC}$ or GND	
lozt	Maximum I/O Leakage Current	3.6		±0.3	±3.0	μΑ	$V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.5	0.8		V	(Notes 2, 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.5	-0.8		V	(Notes 2, 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0		V	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8		V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75 Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVQ245		74LV	Q245	
Symbol	Parameter	V _{CC} (V)		T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Min Typ Max	Min	Max			
t _{PHL} , t _{PLH}	Propagation Delay	2.7 3.3 ±0.3	2.0 2.0	9.0 7.5	14.0 10.0	2.0 2.0	15.0 10.5	ns
tpzL, tpzH	Output Enable Time	2.7 3.3 ±0.3	3.0 3.0	10.2 8.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	2.7 3.3 ±0.3	1.0 1.0	10.2 8.5	20.4 14.5	1.0 1.0	21.0 15.0	ns
toshl,	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

OC Electrical Characteristics (continued)

Symbol	Parame	ter and	Тур	Units	Conditio	ns		
C _{IN}	Input Capacitance Input/Output Capacitance		4.5	pF	V _{CC} = Open V _{CC} = 3.3V			Symbol
C _{I/O}			15	pF			Paramotor	
C _{PD} (Note 1)	Power Diss Capacitano				loro			
Note 1: C _{PD} is me	asured at 10 MHz.						Output Current	
HD = 2.0V Min		88-				3.6		
= Vec			4	4.6		3.6	Maximum Quiescent Supply Curent	90
$000 = V_{10}, V_{10}$ = $V_{00}, 000$ = $V_{00}, 000$		3.0		\$,0±		3,6	Naximum I/O Leakage Current	120
tes 2, 3)	V (No			8.0		3.3	Quiet Output Maximum Dynamic Vot.	/OLP
	old) V				a.o-	9.3	Quiet Output Minimum Dynamic Vol.	
	oVI) V				1.6		Maximum High Level Dynamic Input Voltage	ані,
	ol4) v			8.0		8.8	Maximum Low Level Dynamic Input Voltage	

tiviaximum test duration 2.0 ms, one output loaded at a time.

Note 1: Indident wave sufficing on transmission lines with intradences as low as 75th for communical transportative range is guaranteed for 74LVO.

Note 2: Worst case package.

Note & Max number of outputs defined as (n). Date inputs are driven 0V to 3.3V; one output at GMD.

Note 4: Max number of Dails Include (in) switching, (n - 1) inputs switching 3.3%. Imputsmost hast switching: 3.3% to threshold $(V_{E,D})$, 6V to threshold

AC Electrical Characteristics: See Seetion 2 for Test Methodology

	0246	74LV		74LVQ245					
ctinú	- 40°C 88°C 50 pf	+ 01		r _A = +25°C C _L = 50 pF		ooV (V)	Paramoter	Symbol	
	KBM	nilli		Typ	Meles				
an	15.0 10.6	0.9 0.8	14.0 10.0	9.0	2.0 2.0	2.7 3.3 ± 0.3			
	19.0 13.5	3.0	16.3			2.7 3.8 ±0.8	Output Enable Time	संदर्भ गरक	
	21.0	0.1	20,4			2.7 3.8 ± 0.5	Output Disable Time	Endy "ZHdg	
	1.5		1.5	1.0		2.7	Output to Output Skew*		

Slow is defined as the absolute value of the difference between the actual propagation dusty for any tage superate employs on the same ultestion, either HiGH to COW (topsa). Or LOW to HIGH (logge). Parameter guaranteed by design.





74LVQ273 Low Voltage Octal D Flip-Flop

General Description

The LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

■ Ideal for low power/low noise 3.3V applications

Absolute Maximum Ratings (vots)
If Miliary/Aerospace specified devices are required,
please contact the Netional Semiconductor Sales

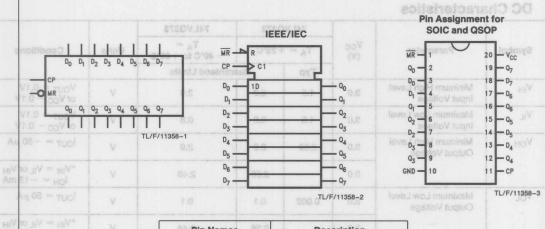
- Implements patented Quiet Series EMI reduction Circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Ordering Code: See Section 11

Logic Symbols

 $V_1 = V_{CC}$, GND

Connection Diagram



Pin Names 88.0	Description
D ₀ -D ₇	Data Inputs
0.1 D ₀ -D ₇	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

	SOIC JEDEC	SOIC	SSOP JEDEC
Order Number	74LVQ273SC 74LVQ273SCX	74LVQ273SJ 74LVQ273SJX	74LVQ273QSC 74LVQ273QSCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Vcc) -0.5V to +7.0VDC Input Diode Current (IIK)

 $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA -0.5V to $V_{CC} + 0.5V$

DC Input Voltage (Vi) DC Output Diode Current (IOK)

Vo = -0.5Vggs VC.C esion wolvewood wol tot I=20 mA Vo = Vcc + 0.5Veened telu0 betneted atnemet 20 mA

±50 mA

DC Output Voltage (Vo) -0.5V to Vcc + 0.5V DC Output Source

or Sink Current (IO) M Guaranteed simultane DC V_{CC} or Ground Current

Am 04 ± 400 mA (Icc or IGND) -65°C to +150°C Storage Temperature (TSTG)

DC Latch-up Source or

Sink Current ±300 mA

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (Vcc) LVQ

2.0V to 3.6V

Input Voltage (V_I)

OV to VCC OV to Vcc

Output Voltage (Vo) Operating Temperature (T_A) 74LVQ

-40°C to +85°C

Minimum Input Edge Rate ΔV/Δt V_{IN} from 0.8V to 2.0V

V_{CC} @ 3.0V

The register is fully edge-triggered. The state of each D insition, is transferred to the corresponding flip-flop's Q out-

Clock (CP) and Master Reset (MR) Input load and reset

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The

Ordering Code: See Section 11

Logic Symbols

DC Characteristics

90	SOIC and QS		74LV	Q273	74LVQ273			
Symbol	Parameter	V _{CC} (V)	T _A =	+ 25°C	T _A = -40°C to +85°C	Units	Conditions	
40	0,-2		Тур	Gua	aranteed Limits	Su 10 So Zo		
VIH TO T	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{IL} 8	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V _{OH} Q - E	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
90 00 11	OI GNO	3.0		2.58	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$	
e-V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		3.0	Dos	0.36	pame# ni 0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
I _{IN}	Maximum Input Leakage Current	3.6	Data ir Master	±0.1	₹ ^Q -0 ^Q ## 1.0	μА	$V_{I} = V_{CC}$, GND	

^{*}All outputs loaded; thresholds on input associated with output under test.

9088	SOIC	SOIC	
74LVQ273QSC 74LVQ273QSCX	74EVG273SJ 74LVG273SJX	74LVQ273SG 74LVQ273SCX	Order Number
MCA20		M20B	See NS Package Number

Symbol	Parameter	Vcc (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions	
	$C_{L} = 50 \text{ pF}$		Тур	Guara	anteed Limits			
IOLD	†Minimum Dynamic Output Current	3.6	dAı	2.7	36 OJ 10 H	mA a	V _{OLD} = 0.8V Max (Note 1)	
I _{OHD}	0,0	3.6		7.5	-25/OJ 10 t	DIH MA _I T	V _{OHD} = 2.0V Min (Note 1)	
Icc	Maximum Quiescent Supply Current	3.6		4.0	40.0	μА	$V_{IN} = V_{CC}$ or GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	7 3.3	0.4	0.8	3.0	Puls VMidth	(Notes 2, 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.3	-0.8	E.B	overyTime o CP	(Notes 2, 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		٧	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	neter 1	Was V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package,

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVQ273		74LV	Q273	
Symbol	Parameter	V _{CC} (V)		T _A = +25°C C _L = 50 pF		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$		Units
			Min	Тур	Max	Min	Max	
f _{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	50 90			45 75		MHz
t _{PLH}	Propagation Delay CP to Q _n	2.7 3.3 ±0.3	4.0 4.0	9.6 8.0	17.6 12.5	3.0 3.0	20.0 14.0	ns
t _{PHL}	Propagation Delay CP to Q _n	2.7 3.3 ±0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.5 14.5	ns
t _{PHL}	Propagation Delay MR to Qn	2.7 3.3 ±0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.0 14.0	ns
toshl,	Output to Output Skew*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements: See Section 2 for Test Methodology unifned additional and a section 2 for Test Methodology unifned additional and a section 2 for Test Methodology unifned and 2 for Test Methodology unifned and 2 for Test Methodology unifned a section 2 for Test M

			HLVQ273	73 7	OV.INT 74LV	/Q273	74LVQ273	
Symbol	:0	Parameter 38 + 01 3		(v) CL - 50 pr			T _A = -40°C to +85°C C _L = 50 pF	Units
V657 V0.0	11		SHMTS	Guaranteed	Тур	Guara	anteed Minimum	
t _s (1	Setu D _n to	p Time, HIGH	or LOW	2.7 3.3 ±0.3		6.5 5.0	8.5 6.0	ns
th (1	Hold D _n to	Time, HIGH o	or LOW -	2.7 3.3 ±0.3		0.0 0.0	0.0 0.0	ns
t _w		k Pulse Width H or LOW	40.0	2.7 3.3 ±0.3		8.8 7.0 5.5	8.5 6.0	ns
t _w	MH	Pulse Width H or LOW		2.7 3.3 ±0.3	0.4	8.8 7.0 5.5	8.5 8.5 6.0 8.5 6.0	ns
t _w (ε,s:	Heck	overy Time to CP		2.7 3.3 ±0.3	0.0-	8.8 5.0 4.0	6.5 feiuO omeny 4.5 miniM	ns

Capacitance

Symbol	Parameter	Typ 8.0	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	se 750 for comment 35	wol en seonsbegr pF	V _{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Note 4: Max number of Data Inputs (n) switching, (n-1) inputs switching OV to 3.3V, input-under-test switching: 8.5V to 10

		ATEL		74LVQ273				
= -40°C +85°C Units = 50 pF	+ oi	T _A = +25°C O _L = 50 pF		Vac (V)	Parameter	Symbol		
	xsM			тур				
							Maximum Clock Frequency	fmax.
ns		3.0 3.0	17.6 12.5	9.6 0.8	4.0		Propagation Delay CP to Qn	Frid
		3.5 3.5	18,8		4.0	2.7 2.3 ±0.3	Propagation Delay CP to Q _n	THd
	20.0 14.0	3.5 3.5		10.2	4.0	2.7 3.3 ± 0.3	Propagation Delay MR to Q ₀	ТРЫГ
su	1.6		1.5			2.7 3.3 ±0.3	Output to Output Skew*	FOSTH COSTH

*Skaw is defined as the abopting value of the difference between the soluted propagation delay for any two outputs within the same packaged device. The appointment of the same disorbion, either HIGH to LOW to HIGH (togst). Parameter guaranteed by dealer. Not



74LVQ373

Low Voltage Octal Transparent Latch it notismoin eith erit sential erit WOJ with TRI-STATE® Outputs -noo ess attuquo brabasta STATE-617 eti Jonobise

General Description

The LVQ373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

Features in etate 2 edit ni ena atuquo bishnete edit

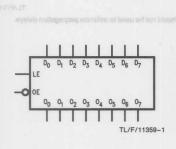
- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

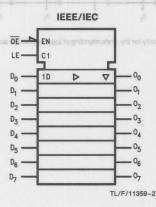
Ordering Code: See Section 11

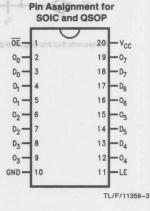
Logic Symbols

Connection Diagram

Functional Description







Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
ŌĒ	Output Enable Input
00-07	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ373SC 74LVQ373SCX	74LVQ373SJ 74LVQ373SJX	74LVQ373QSC 74LVQ373QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

The LVQ373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable (OE) input. When OE is LOW, the standard outputs are in the 2-state mode. When OE is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the

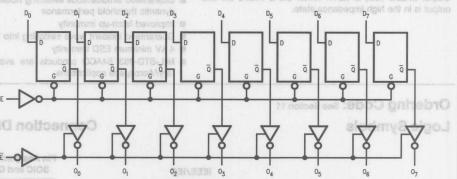
Truth Table

	Inputs					
LE	ŌĒ	Dn	On			
X	Н	X	Z Z			
- Harry	1000 Lat 19 10	and sta	a Louis			
H	113750	A.H.	A AA How			
tuctue	DOGTA	X	00			

- H = HIGH Voltage Level
- L = LOW Voltage Level
- Z = High Impedance note! Iniple to statence EYEQVI edT
- X = Immaterial

O₀ = Previous O₀ before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/11359-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) -0.5V to +7.0V DC Input Diode Current (I_{IK}) $V_{I} = -0.5V$ -20 mA ac + 20 mA $V_1 = V_{CC} + 0.5V$

DC Input Voltage (V_I) -0.5V to $V_{CC} + 0.5V$ DC Output Diode Current (IOK)

 $V_0 = -0.5V$ 0.04 -20 mA $V_{O} = V_{CC} + 0.5V$ +20 mA DC Output Voltage (Vo) -0.5V to V_{CC} + 0.5V DC Output Source

or Sink Current (Io) DC V_{CC} or Ground Current (ICC or IGND) Storage Temperature (TSTG)

DC Latch-Up Source or Sink Current

The "Recommended Operating Conditions" table will define the conditions for actual device operation, we follow more of the same as a company of the same relative sent notes in a principle of the same relative sent notes in

Recommended Operating Conditions

Parameter Supply Voltage (Vcc) 2.0V to 3.6V LVQ Input Voltage (V_I) OV to VCC Output Voltage (Vo) OV to Vcc

Operating Temperature (TA)

-40°C to +85°C 74LVQ Minimum Input Edge Rate (ΔV/Δt)

DC Electrical Characteristics (continued)

VIN from 0.8V to 2.0V

STATE-IFT mumical 125 mV/ns Vcc @ 3.0V

±300 mA Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings.

DC Characteristics

	An '(CTIA) mouseum of Arm thi	NOUNE ISSI-	74LV	Q373	74LVQ373	We in sought an	Conditions	
Symbol	Parameter	V _{CC} (V)	= AT	+ 25°C	T _A = -40°C to +85°C	Units		
	7AL VOS23		Тур	Typ Guarant				
VIH	Minimum High Level Input Voltage	3.0	1.5_ A	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
VIL	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
VOH	Minimum High Level	3.0	2.99	2.9	2.9	velor Violite	$I_{OUT} = -50 \mu\text{A}$	
an	Output Voltage	3.0	0.8	2.58	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$	
VOL	Maximum Low Level	3:0	0.002	0.1	€.0 ± €0.1	V	$I_{OUT} = 50 \mu\text{A}$	
	Output Voltage	3.0	10.2 8.5	0.36	7.8 0.44 6.0± 8.8	Enalys Time	$^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$	
ING	Maximum Input Leakage Current	3.6	10.8	±0.1		emit eldesic	$V_{I} = V_{CC}$, GND	

±50 mA

-65°C to +150°C

±400 mA 8.0

"Slow is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HTGH to LOW (togget) or LOW to RIGH (togget). Persmater guaranteed by design

^{*}All outputs loaded; thresholds on input associated with output under test.

2.CV to 3.6V		(V) =	silov' Aqqu	1200 V	to +85°C	Units	Conditions
		/ to	Тур	Guar	Guaranteed Limits		DC Input Diode Current (lat)
lold	†Minimum Dynamic	3.6	alloV fuch	0 4	108+ 36	mA	V _{OLD} = 0.8V Max (Note 1)
IOHD	Output Current	3.6	perating To	0 1	4.0 + 0 0 25 Va.0	mA	V _{OHD} = 2.0V Min (Note 1)
Icc	Maximum Quiescent Supply Current	3.6	r4LVQ inimum Inp	4.0	03-40.0	μА	V _{IN} = V _{CC} or GND
loz\Vm 83	Maximum TRI-STATE Leakage Current	3.6	V _{CC} @ 3.01	±0.25	±2.5	μΑ	$V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8	± 400 nu	V	(Notes 2, 3) TO 30 V DO (QUAL TO 30)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.3	-0.8	7061 + G10°68 -	٧	(Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	s" are those value cannot be guard	um Veting the device	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	f at those limits. The ical Characteristics is anaximum cetin in	the Operated the Viector	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ. Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

DC Characteristics Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold

The "Recommended Operating Conditions" table will define

Parameter

AC Electrical Characteristics: See Section 2 for Test Methodology

		attenil beams	54/67	74LVQ373		74LVQ373	
Symbol	Parameter	0.S V _{CC}	0.8	T _A = +25°C	9.0	T _A = -40°C to +85°C	Units
V1.0 =	Tuo ^V	8.0 (V)	8.0	C _L = 50 pF	0.0	OVEL CL = 50 pF	ViL
V1.0 -	00 V 10		Min	Тур	Max	Min Max	
t _{PHL} ,	Propagation Delay Dn to On	2.7 3.3 ±0.3	2.5 2.5	9.6 8.0	14.8 10.5	2.5 16.0 2.5 11.0	ns
t _{PLH} ,	Propagation Delay LE to O _n	2.7 3.3 ±0.3	2.5 2.5	9.6	16.9 12.0	2.5 18.0 2.5 mum 12.5	ns
tpZL,	Output Enable Time	2.7 3.3 ±0.3	2.5 2.5	10.2 8.5	18.3 13.0	2.5 19.0 2.5 13.5	ns
t _{PHZ} , 00 t _{PLZ}	Output Disable Time	2.7 3.3 ±0.3	1.0	10.8 9.0	20.4 14.5	1.0 d mumi 21.0 11.0 O está 15.0	ns
toshl,	Output to Output Skew*	2.7 3.3 ±0.3		1.0 region	1.5	oces fugni no oblorizenti 1,5000 c 1.5	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshi) or LOW to HIGH (toshi). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology	Inanidately .
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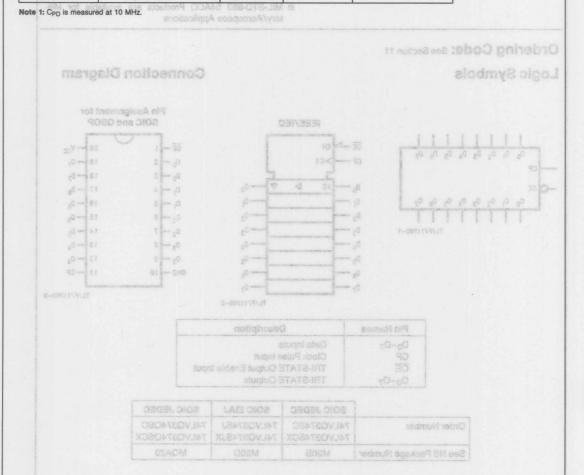
M Guaranteed simultaneous switching noise level and dy-

			74LV	Q373	74LVQ373	o Maria
Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
	-STATE® Output	IAT dilw	Тур	Guaran	Guaranteed Minimum	
ts	Setup Time, HIGH or LOW	2.7 3.3 ±0.3	0	4.0 3.0	4.5	ns
t _H	Hold Time, HIGH or LOW	2.7 3.3 ±0.3	g 0 qoff-	1.5	is a hig 3.poed, low separa 3.P-type inp	The LVQ374 flop seturing
tw	LE Pulse Width, HIGH	2.7 3.3 ±0.3	2.4	5.0 4.0	4.0)) xloons bere

Capacitance

Symbol	Parameter Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	TRI-STATE out	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.





74LVQ374

Low Voltage Octal D Flip-Flop with TRI-STATE® Outputs

79

TA = +25°C

 $C_1 = 50 \text{ pF}$

General Description

The LVQ374 is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops.

Conditions

Features

Vec

■ Ideal for low power/low noise 3.3V applications

AC Operating Requirements: See Section 2 for Test Methodology

- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance Capacitance

Parameter

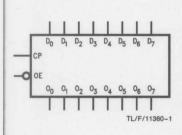
Symbol

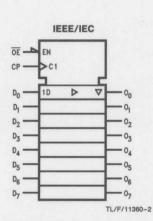
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- MIL-STD-883 54ACQ Products are available for Military/Aerospace Applications

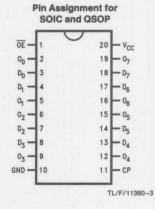
Ordering Code: See Section 11

Logic Symbols

Connection Diagram







	Pin Names	Description
	D ₀ -D ₇	Data Inputs
	CP	Clock Pulse Input
- 1	ŌĒ	TRI-STATE Output Enable Input
	00-07	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	SOIC JEDEC
Order Number	74LVQ374SC 74LVQ374SCX		74LVQ374QSC 74LVQ374QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

The LVQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flipflops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

Truth Table 199 mumixs M stulosdA

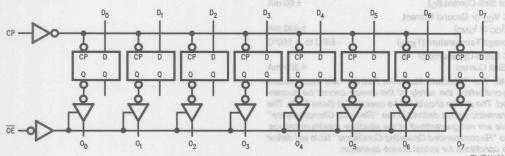
betiuper en	Inputs	Hoogs specific	Outputs
Dn	CP	OE of a	otudisiOn\aciti
8V toH 7.0		L 6	V) egatiHV ylqqu
L	_	(NE) Inem	C Input_Diode Cu
m X	X	Н	VI = Z0.6V

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Z = High Impedance = LOW-to-HIGH Transition

Logic Diagram



TL/F/11360-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

		74LVQ374	3874			
Conditions		Vcc TA = +25°C -40°C to +55°C Unit		Paramoter	Symbol	
					Minimum High Lovel Input Voltage	HIV
$V_{OUT} = 0.1V$ or $V_{CO} = 0.1V$						
					Minimum High Level	
$V_{\rm IM} = V_{\rm IL}$ or $V_{\rm IM} = V_{\rm IM} = -12$ mA	V				Output Voltage	
	V					
		0.44			Output Voltage	
						vu ¹

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Diode Current (I _{IK}) $V_{I} = -0.5V$ $V_{I} = V_{CC} + 0.5V$	−20 mA +20 mA
DC Input Voltage (V _I)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	−20 mA +20 mA
DC Output Voltage (V _O)	-0.5 V to $V_{CC} + 0.5$ V
DC Output Source or Sink Current (I _O)	±50 mA
DC V _{CC} or Ground Current	± 400 mA

Storage Temperature (T_{STG}) -65°C to +150°C

DC Latch-Up Source or

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define

the conditions for actual device operation.

Sink Current

Recommended Operating

outs and TRI-STATE rue outputs, The	
Supply Voltage (V _{CC})	2.0V to 3.6V
Input Voltage (VI) cutes and team tent	engni o OV to Vcc
Output Voltage (Vo)	Jedino OV to Vcc
Operating Temperature (T _A) WOJ (30)	-40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt) V _{IN} from 0.8V to 2.0V	OE input does not a
V _{CC} @ 3.0V	125 mV/ns

DC Electrical Characteristics

			74LV	Q374	74LVQ374		
Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C	Units	Conditions
			Тур	Gua	ranteed Limits		
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		3.0		2.58	2.48	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
	Output Voltage	3.0		0.36	0.44	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	μΑ	$V_{I} = V_{CC}$, GND

±300 mA

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Electrical Characteristics (Continued) is noticed and testinementupe A pritisage OA

	74LVQ374	74LVQ374		74LVQ374				
Symbol	Parameter	V _{CC} (V)	= ATTA = +25°C 00		T _A = -40°C to +85°C	Units	Conditions	
	CL = 50 pF		Тур	Guara	anteed Limits			
lold	†Minimum Dynamic Output Current	3.6	Typ 0	2.7	36 WOJ 10 HD	MA Ip Time, H	V _{OLD} = 0.8V Max (Note 1)	
I _{OHD}	3.0	3.6	0	3 ± 0.3 2.7	-25 WOJ 10 H	o CP Am Time, Hit	V _{OHD} = 2.0V Min (Note 1)	
lcc	Maximum Quiescent Supply Current	3.6	2,4	4.0 4.0 7.S	40.0	ο OP μΑ Pulse Widt	V _{IN} = V _{CC} or GNE	
loz	Maximum TRI-STATE	4,0	2.0	8 ± 0.3	.8	H or LOW	$V_{I}(OE) = V_{IL}, V_{IH}$	
	Leakage Current	3.6		±0.25	±2.5	μΑ	$V_I = V_{CC}$, GND $V_O = V_{CC}$, GND	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.5	0.8		V	(Notes 2, 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	oV3.3	-0.3	-0.8	epacitance	D fue V i	(Notes 2, 3)	
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	Jiesipation ance	Power (Vipacit	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75 Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

				74LVQ374	1	74LV	Q374	
Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF			$T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$		Units
			Min	Тур	Max	Min	Max	
f _{max}	Maximum Clock Frequency	2.7 3.3 ±0.3	55 75			50 70		MHz
t _{PLH} , t _{PHL}	Propagation Delay CP to On	2.7 3.3 ±0.3	3.0 3.0	11.4 9.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t _{PZL} , t _{PZH}	Output Enable Time	2.7 3.3 ±0.3	3.0 3.0	11.4 9.5	18.3 13.0	3.0 3.0	19.0 13.5	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	2.7 3.3 ±0.3	1.0 1.0	11.4 9.5	20.4 14.5	1.0 1.0	21.0 15.0	ns
toshl,	Output to Output Skew* CP to On	2.7 3.3 ±0.3		1.0 1.0	1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

Symbol	Parameter V _{CC} (V)		T _A = +25°C C _L = 50 pF		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$	Units
xaM V8.0 =	noV . Voice		Тур	Guaranteed Minimum		0.10
t _S	Setup Time, HIGH or LOW	2.7	0	4.0	Iner 4.5 tugtuO	
niM VO.S =	D _n to CP	3.3 ±0.3	0	3.0	3.0	ns
t _H (f	Hold Time, HIGH or LOW	2.7	0	1.5	1.5	
Ven of GNE	D _n to CP	3.3 ±0.3	0	1.5	Hansaiu 01,5 mixeM	ns
t _W	CP Pulse Width,	2.7	2.4	5.0	Supply 0.6 rent	
μV , $\mu V = G$	HIGH or LOW	3.3 ±0.3	2.0	4.0	Maximu 0.4 PILSTATE	ns
Vac GND	= N Au Bos	20 n-i		1 20	Looked Camping I	

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.580-	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	39 0.5	pF	V _{CC} = 3.3V

Note 1: CPD is measured at 10 MHz.

Twestmum test duration Z.O ma, one curput logget et a arriv.

Note: It incident wave switching on transmission thes with impedances as low as 75th for commercial temperature range is guaranteed for 74LVQ.

lote 2: Worst case package.

Radio 61 Acax number of Data (npx)s and other or 1) inputs switching: 0.3V. Input-undertest switching: 8.3V to threshold (V_{ILD}), OV to threshold

AC Electrical Characteristics: See Section 2 for Test Methodology

Maximum Low Level

	76LV0376 TA = -40°C 10 +65°C CL = 80 pF		TA = +25°C TA = -40°C					
						Parameter		
		nitt		GYT	nise			
sHM						2.7 3.3 ± 0.3	Masdmum Clook Frequency	
	19.0			9.5		2.7 3.8 ±0.3	Propagation Delay CP to On	
	19.0		18.8	11,4 9.5			Output Enable Time	PZ4
an	21.0 15.0	1.0	20.4	11,4		2.7 3.3 ± 0.3		(eHZ)
			1.5				Output to Output Skew* CP to On	товин товин

*Stays is defined as the absolute value of the difference between the coluct propagation delay for any two expects outputs of the same device. The specifies to any outputs evidation in the same decessor, exists fallow though out LOW to HIGH (box ut). Percentage outputs of the same decessor, exists fallow to LOW to HIGH (box ut). Percentage output of the same decessor, and other than the same decessor.



the latches are transparent, i.e., a latch output will change 74LVQ573 state each time its D input changes. When LE is LOW the Low Voltage Octal Latch with TRI-STATE® Outputs

General Description

The LVQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs. The LVQ573 is functionally identical to the LVQ373 but with inputs and outputs on opposite sides of the package.

abled. When OE is HIGH the buffers are ■ Ideal for low power/low noise 3.3V applications

The LVQ578 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition

- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP pack-
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Ordering Code: See Section 11

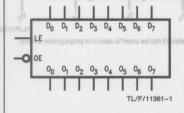
Logic Symbols

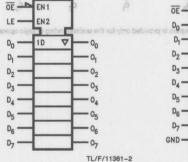
Connection Diagram

Functional Description

Enable (OE) Input, When OE is LO









Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
ŌĒ	TRI-STATE Output Enable Input
00-07	TRI-STATE Latch Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ573SC 74LVQ573SCX	74LVQ573SJ 74LVQ573SJX	74LVQ573QSC 74LVQ573QSCX
See NS Package Number	M20B	M20D	MQA20

Functional Description

The LVQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are enabled. When OE is HIGH the buffers are in the high impedance mode but this does not interfere with entering new Z = High Impedance data into the latches. The 2 tolub between etnemelors we

Truth Table

	Inputs					
ŌĒ	LE	D	On			
L	Н	eHe sa	AND BHE			
L	Н	C res	2 A - 12 SE #			
riota l	18140	TO X O	00			
Н	X	X	Z			

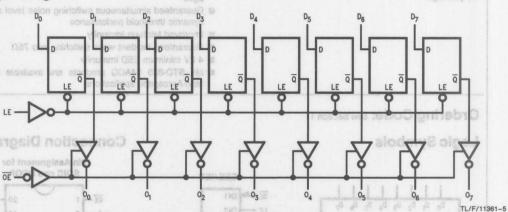
H = HIGH Voltage

L = LOW Voltage

X = Immaterial

O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Description

SSOP JEDEC	SOICEIAL	SOIC JEDEC	
74LVQ573QSC 74LVQ573QSCX	74LVQ573SJ 74LVQ573SJX	74LVQ6738C 74LVQ873SCX	Order Number
OSAOM	MSDD		See NS Package Number

Office/Distributors for available Supply Voltage (V _{CC}) DC Input Diode Current (I _{IK})	-0.5V to +7.0V	LVQ Input Volta Output Vol		.Parameter	2.0V to 3.6V 0V to V _{CC} 0V to V _{CC}
$V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage (V _I)	-20 mA +20 mA -0.5V to V _{CC} + 0.5V	74LVQ	9.6	ture (T _A) manual muminiM1	°C to +85°C
DC Output Diode Current (I _{OK}) V _O = -0.5V	∂\$20 mA		0.8V to	e Rate (ΔV/Δt) 2.0V	125 mV/ns
$V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O)	+20 mA -0.5V to V _{CC} + 0.5V		8.6	Maximum Quiescent Supply Current	00
DC Output Source or Sink Current (I _O) DC V _{CC} or Ground Current (I _{CC} or I _{GND})	±50 mA ±50 mA ±400 mA		3.6	Maximum TRI-STATE Leakage Curent	20
Storage Temperature (T _{STG}) DC Latch-Up Source or	-65°C to +150°C	8.0		Quiet Output Maximum Dynamie Vol.	VOLP
Sink Current Note: The "Absolute Maximum		4.0	8.8	Quiet Output Minimum Dynamic V _{OL}	
beyond which the safety of the teed. The device should not be of parametric values defined in the	operated at these limits. The	1.6	8.6	Maximum High Leval Dynamic Input Voltage	
table are not guaranteed at the The "Recommended Operating the conditions for actual device	Conditions" table will define	1.6	3.8	Maximum Low Level Dynamic Input Voltage	VII.D

DC Electrical Characteristics

		74LVQ573 74I		74LVQ573	ge. Hould defined ab	Note 2: Worst case packs Note 3: Max number of o	
Symbol	Parameter Parameter	V _{CC} (V)	T _A = -	- 25°C	T _A = -40°C to +85°C	Units	Conditions
		vgolobon	Typ Guaranteed Limits		I Chara	AC Electrica	
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
VIL	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	Partymeter	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
VoH	Minimum High Level	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
en	Output Voltage	3.0	.5 10	2.58	2,48	agnii V r Dela	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
VOL	Maximum Low Level	3.0	0.002	0.1	0.1	to C V	I _{OUT} = 50 μA
	Output Voltage	3.0	8 81 04 7.0	0.36	0.44	V nOt	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
IIN	Maximum Input Leakage Current	3.6	8 33	± 0.1	± 1.0	μΑ	$V_{I} = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

Slave is defined as the electute value of the difference between the actual proprigation delay for any two separate outputs of the earns device. The specification applies to any outputs evidenting in the same direction, either HIGH to LOW flogge, or LOW to HIGH (1984). Parameter guaranteed by design.

Symbol/	Parameter	V _{CC} (V)	T _A = +25°C T _A = -40°C to +85°C				to toution seeding strotted to the conditions (Conditions)
OV to Voc		tage (Vo)	V Тур.		ranteed Limits	(50l) Inc	DC Input Diode Curre
Octo + 85°C	†Minimum Dynamic T) 914 Output Current	3.6	Operating 74LVQ	Am Va.c	30	mA	V _{OLD} = 0.8 V _{Max} (Note 1)
IOHD	PRate (AVVAt) 2.0V	0 3.6.0	Minimum I V _{IN} fron	Am	-25	(Mana)	V _{OHD} = 2.0V V _{Min} (Note 1)
lcc	Maximum Quiescent Supply Current	3.6		4.0/8.0	+ 00V 040.00-	μΑ (ο	$V_{IN} = V_{CC}$ or GND
loz	Maximum TRI-STATE Leakage Curent	3.6		± 0.25	±2.5	μΑ	$V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8	-65°C to +1	(SysT)	(Notes 2, 3) and 2
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	-0.8	±304 Ratings" are those va	MaXmum	(Notes 2, 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0	perated at these limits "Electrical Character's	ined in the a	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	absolute maximum reli Conditions" table will d obecation	leed at the Op∈ V ubing i tual davice	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

VI.0 - 0.1V	TUOV	V	0.8	0.5	3	74LVQ573	lov	74LV	Q573	HIV
Symbol		Parameter	8.0	V _{CC} (V)	3	T _A = +25°C C _L = 50 pF	level	to +	-40°C 85°C 50 pF	Units
= -50 µА	TUOI	V	8.8	8.5	Min	Тур	Max	Min	Max	ноУ
t _{PHL} ,	to a complete	pagation Delay to O _n	2.48	2.7 3.3 ±0.3	2.5 2.5	10.2 0.8 8.5	14.8 10.5	2.5 2.5	16.0 11.0	ns
t _{PLH} ,		pagation Delay to O _n	5.0	2.7 3.3 ±0.3	2.5 2.5	10.2	16.9 12.0	2.5 2.5	18.0 12.5	ns
t _{PZL} ,	1000	put Enable Time	-10	2.7 3.3 ±0.3	2.5 2.5	10.2 8.5	18.3 13.0	2.5 12.5	19.0	ns
t _{PHZ} ,	Out	put Disable Time		2.7 3.3 ±0.3	1.0	10.8	20.4	1.0	21.0 15.0	ns shuqtuo HA
toshl,		put to Output Ske	w*	2.7 3.3 ±0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

^{*}Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Test Methodology

			74LV	Q573	74LVQ573	
Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$	Units
			Тур	Guara	inteed Minimum	
ts	Setup Time, HIGH or LOW D _n to LE	2.7 3.3 ±0.3	0	4.0 3.0	4.5 3.0	ns
t _H	Hold Time, HIGH or LOW D _n to LE	2.7 3.3 ±0.3	0	1.5 1.5	1.5 1.5	ns
t _W	LE Pulse Width, HIGH	2.7 3.3 ±0.3	2.4 2.0	5.0 4.0	6.0 4.0	ns

Capacitance

Symbol	Parameter	Тур	Units	Conditions
CIN	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 1)	Power Dissipation Capacitance	37	pF	V _{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

AC Operating Requirements: See Section 2 for Test Methodology

	T APPROVE IN FE	T. Comme				
on Unite	74LV0578	74LVQ573				
	TA = -40°C to +85°C CL = 50 pF	4	$T_A = +$ $G_L = 1$	00 ^V . (V)	Parameter	
	muminiM been	Guaran	qyT			
		4.0	0		Setup Time, HIGH or LOW D _n to LE	
	1.5	1.5		2.7 3.3 ± 0.3	Hold Time, HIGH or LOW Dn to LE	H
	6.0	5,0	2.4	2.7 3.5 ± 0.3	LE Pulse Width, HIGH	W

Capacitance

Conditions	Units	Typ	Parameter	
V _{OC} = Open		4.5	Input Capacitance	
$V_{OC} = 3.3V$	₹q	76	Power Dissipation Capacitance	C _{PD} (Note 1)

Note 1: CPD is measured at 10 MHz.



Section 10 Contents

10-0	LVT Family Features
10-4	74LVT125 3.3V ABT Quad Buffer with TRI-STATE Outputs
10-6	74LVT240 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs
10-6	74LVT244 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs
10-10	74LVT245 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs
10-14	74LVT373 3.3V ABT Octal Transperent Latch with TRI-STATE Outputs
10-16	74LVT374 3.3V ABT Octal D Flip-Flop with TRI-STATE Outputs
10-18	74LVT646 3.3V ABT Octal Transceiver/Register with TRI-STATE Outputs
10-20	74LVT652 3.3V ABT Octal Tr 01 noitoeS with TRI-STATE Outputs
	74LVT16240 3.3V ABT 16-Bit Inverting Burler/Line Driver with TRI-STATE Outputs
	74LVT16244 3.3V ABT 16-Wime Ant Versith TRI-STATE Outputs
10-27	74LVT16244 3.3V ABT 16-VilmaFaTVM with TRI-STATE Outputs 74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE Outputs
10-29	74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs
10-31	74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs
10-33	74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs
10.38	74! VT16652 3 3V AST 16-Rit Transceiver/Register with TRLSTATE Outputs

Section 10 Contents

LVT Family Features	10-3
74LVT125 3.3V ABT Quad Buffer with TRI-STATE Outputs	10-4
74LVT240 3.3V ABT Octal Buffer/Line Driver with TRI-STATE Outputs	10-5
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74LVT245 3.3V ABT Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs	10-10
74LVT373 3.3V ABT Octal Transparent Latch with TRI-STATE Outputs	10-14
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74LVT16373 3.3V ABT 16-Bit Transparent Latch with TRI-STATE Outputs	10-29
74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE Outputs	10-31
74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-33
74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE Outputs	10-36





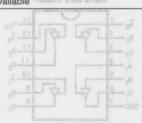
General Description

74LVT125

LVT Family Low Voltage High Speed BiCMOS Logic

Features

Bus Hold data inputs elimines Features	Advantages misch ous entitled seadT	
Extended V _{CC} range from 2.7V to 3.6V, compatible with JEDEC Std. No. 8-1B	Fully characterized for unregulated battery operation and solly observed and street and the months via solly	
State-of-the-Art sub-micron BiCMOS process with special low voltage enhancements	3.3V logic family with equivalent performance of 5V ABT logic family; Propagation delays as fast as 4 ns	
Available in SOIG JEDEG, SOIC EIAJ a vritiuraio agatloV-bexiM Functionally compatible with the 74 series 125	SV tolerant inputs and outputs provide direct interface with standard 5V buses and 5V devices	
+64 mA/-32 mA drive current	Drives large loads, buses, or memory arrays	
Bus-hold circuitry	Eliminates external pullup or pulldown resistors on I/O pins that are being unused or floating	
Power Up/Down TRI-STATE®	Guaranteed glitch-free bus interface during Power Up/Down cycle; Guaranteed Live (Hot) Insertion	
SOIC, EIAJ-SOIC, and TSSOP packaging	Saves board space and weight; TSSOP compatible with PCMCIA standards	
Alternate source available 9022T bns 0102	Product standardization. Ensured product supply	





eldsT diurT

Output			gni
	On	En	
	J	J	
	H	B	
	Z	X	

H = RIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immeterial

	Des	
ATE Outputs		

TSSOP	SOIC EIAJ	SOIC JEDEC	
74LVT125MTCX	74LVT125SJ 74LVT125SJX	74LVT125M 74LVT125MX	Order Number
MTC14	M14D	AATM	See NS Package Number

74LVT125 3.3V ABT Quad Buffer with TRI-STATE® Outputs

General Description

The LVT125 contains four independent non-inverting buffers with TRI-STATE outputs.

These buffers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT125 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V VCC
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 125
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Pin Names

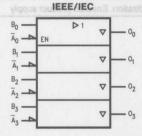
 \overline{A}_n , B_n

On

Logic Symbol

Connection Diagram

Pin Assignment for SOIC and TSSOP

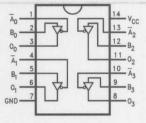


Inputs

Description

TRI-STATE Outputs

TL/F/12011-1



TL/F/12011-2

Truth Table

Inp	uts	Output
An	Bn	On
L	L	L
L	Н	Н
Н	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = HIGH Impedance

X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVT125M 74LVT125MX	74LVT125SJ 74LVT125SJX	74LVT125MTCX
See NS Package Number	M14A	M14D	MTC14

74LVT240 3.3V ABT Octal Buffer/Line of an intermediate of the Control of the Cont

General Description

The LVT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

These octal buffers and line drivers are designed for low-voltage (3.3V) $V_{\rm CC}$ applications, but with the capability to provide a TTL interface to a 5V environment. The LVT240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

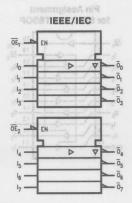
M Lafelyup performance exceeds 500 mA

Features

- Input and output interface capability to systems at 5V VCC
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 240
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

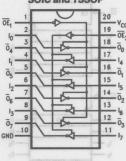
Logic Symbol @ notice and O



TL/F/12012-1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12012-2

Truth Tables

Inputs		Outputs		
OE ₁	E sni9)In	(Pins 12, 14, 16, 18		
L	L	Н		
L	Н	L i		
Н	X	Z		

Inputs		Outputs	
OE ₂	Pleas 12	(Pi	ns 3, 5, 7, 9)
L	L	1	H
L 14	Н	1.5	L
H	X	35	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

Pin Names	Description			
OE ₁ , OE ₂	TRI-STATE Output Enable Inputs			
$\frac{I_0-I_7}{\overline{O}_0-\overline{O}_7}$	Inputs TRI-STATE Outputs			

801	SOIC JEDEC	SOIC EIAJ	TSSOP
Order Number	74LVT240WM 74LVT240WMX	74LVT240SJ 74LVT240SJX	74LVT240MTCX
See NS Package Number	edmuiA	M20D	MTC20

74LVT244

3.3V ABT Octal Buffer/Line Driver 1981 1810 TEA VE.E with TRI-STATE® Outputs 1991 OF TATE-1981 drive 1991 drive 1991 OF TATE-1981 drive 1991 driv

■ Letch-up performance exceeds 500 mA

General Description

The LVT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

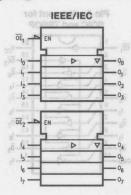
These octal buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 244
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

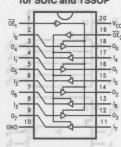
Logic Symbol @ noticenno



TL/F/12014-1

Connection Diagram

Pin Assignment for SOIC and TSSOP



TL/F/12014-2

Truth Tables

Truth Tables

Inputs			Outputs
OE ₁	emare) In	(Pins	12, 14, 16, 18)
L H	L	1	L
L	Н	H	H -
H	X	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial Z = High Impedance

Description
TRI-STATE Output Enable Inputs
Inputs
Outputs

POIGS	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT244WM 74LVT244WMX	74LVT244SJ 74LVT244SJX	74LVT244MTCX
See NS Package	M sea M20B	M20D	MTC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})		-0.5V to +7.0V	
DC Input Voltage (V _I)	Au	-0.5V to +7.0V	
Output Voltage (V _O) Outputs Tri-stated	Ащ	-0.5V to +7.0V	
Outputs Active OOV TO GMD = W		-0.5V to V _{CC}	
DC Output Current (IO)			
Output in LOW State Output in HIGH State, $V_O > V_{CC}$		128 mA 64 mA	
DC Input Diode Current (I _{IK}) V _I < 0		-50 mA	
DC Output Diode Current (IOK) VO <	O Am	81.0 -50 mA	
Storage Temperature Bonge (T)	6	E°C+0 + 150°C	

Storage Temperature Range (T_{STG}) —65°C to +150°C Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage Operating	2.7V to 3.6V
Input Voltage (V _I)	0V to 5.5V
Output Voltage (Vo)	TATE-IATE
Output in Active State Output in "OFF" State	0V to V _{CC} 0V to 5.5V
Minimum Input Edge Rate (Δt/ΔV) $V_{IN} = 0.8V - 2.0V, V_{CC} = 3.0V$	10 ns/V
Free Air Operating Temperature (T _A)	-40°C to +85°C

DC Electrical Characteristics is level against built against the property of t

		000	T _A = -40°C to +85°C		onino	Dynamic Swife
	Parameter O'as		Min	Typ (Note 1) Max	Units	Conditions
V _{IK}	Input Clamp Diode Voltage	2.7	163	-1.2	V	$I_{\parallel} = -18 \text{ mA}$
VIH	Input HIGH Voltage	2.7-3.6	2.0	im Dynamic Vol.	mbæM ja	$V_0 \le 0.1 V$ or
VIL	Input LOW Voltage	2.7-3.6	9.3	8.0 mic Vol.	umlniM h	$V_0 \ge V_{CC} - 0.1V_0$
VOH	Output HIGH Voltage	2.7-3.6	V _{CC} - 0.2	Dynamic Input Vottege	sa. A ub	$I_{OH} = -100 \mu A$
(etoVI) V	2.7	2.4	Dynamic Input Voltage	ensA wo	$I_{OH} = -8 \text{mA}$
		3.0	2.0	Guaranteed parameter, but	V	$I_{OH} = -32 \text{mA}$
V _{OL}	Output LOW Voltage	2.7	gnt V8 at V0 gni	foliwe stugni t -n (0.2)	(a) Vagai	I _{OL} = 100 μA
		2.7	26	0.5	٧	I _{OL} = 24 mA
	dology	3.0	IUI 3 (NUUSEG.)	0.4	٧	I _{OL} = 16 mA
	-49°C to +85°C 50 pF, R _L = 500Ω	3.0		0.5	٧	I _{OL} = 32 mA
aritint)	West of West of The	3.0	W	0.55	V	I _{OL} = 64 mA
I _{I(HOLD)}	Bus-Held Input Minimum Drive	3.0	75		μΑ	V _I = 0.8V
	Max Min Max	(freigh)	-75		μΑ	V _I = 2.0V
I _{I(OD)}	Bus-Held Input Over-Drive	3.0	500	lay Data to Output	μΑ	(Note 2)
1017	Current to Change State		-500		μΑ	(Note 3)
l _{l sn}	Input Current S.8	0 or 3.6	1.0	10	μΑ	V _I = 5.5V
	Control Pins	3.6	0.1	±1	μΑ	V _I = 0V or V _{CC}
80	Data Pins	3.6	8.1	-5	μΑ	$V_I = 0V$
				walsa n	μΑ	$V_I = V_{CC}$
I _{IH} +EII	Control Pin Input Current	3.6		10	μA (S	$V_{CC} \le V_I \le 5.5V$
loff	Input or Output Current	0		○19 =±100 P	μΑ	$0V \le V_1 \text{ or } V_0 \le 5.5$
lozL	TRI-STATE Output Leakage Current	3.6	avean the soluci	ad somewhile and to eulev a	μΑ	$V_O = 0V$

DC Electrical Characteristics (Continued)

	80	OBH	TA = -	40°C to +85°C	Seqlys randitus	If Military/Aerospace specified of please contact the Mailonal S
Symbol	Parameter VT.S	V _{CC} (V)	niM)pen	Typ Max (Note 1)	Units	Office/Disandithoon availability Supply Voltage (Voc)
lozh	TRI-STATE Output Leakage Current	3.6	Jugged	V0.7+ of \6.0	μΑ	$V_{O} = V_{CC}$ (V) $V_{O} = V_{O}$
lozh+	TRI-STATE Output Leakage Current	3.6	Outpu	V0 X + ot 10 o	μΑ	V _{CC} ≤ V _O ≤ 5.5V
ICCH V\an 0	Power Supply Current	3.6	Minimus Vw. =	0.19 Vac Vac	mA	V _I = GND or V _{CC} , evidoA stugitiO Outputs High _{Ol}) manuO tugitiO OO
IccL ³⁸ +	Power Supply Current	3.6	Free Air	Am 851 Am 48 12	mA	V _I = GND or V _{CC} , Outputs Low
Iccz	Power Supply Current	3.6		Am 03- 0.19	mA O	V _I = GND or V _{CC} , outputs Disabled
ICCZH+	Power Supply Current	3.6		equiev e 0.19	mA	$V_I = GND \text{ or } V_{CC}, V_{CC} \le V_O \le 5.5V,$ Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 4)	3.6		"2.0 cteristics" - "	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND

Absolute Maximum Flatings (Note)

The "Recommended Operating Conditions" table will define

Note 1: All typical values are at $V_{CC} = 3.3V$, $T_A = 25$ °C.

Note 2: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 3: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 4: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology (Note 1)

Symbol	Parameter (1 slow)	V _{CC} (V)	TA = 25°C	Units	Conditions $C_L = 50 \text{ pF}, R_L = 500\Omega$	
Symbol	n8t- = d V St-		Min Typ Max			
V _{OLP}	Quiet Output Maximum Dynamic VOL	3.3	8.0, 7-36	V	(Note 2)	
VOLV -	Quiet Output Minimum Dynamic VOL	3.3	8.0 7 7-36	V	(Note 2)	
VIHDALLO	Minimum High Level Dynamic Input Voltage	3.3	27-36	V	(Note 3)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3,3	7.0	V	(Note 3)	

Note 1: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 2: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output at LOW.

Note 3: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{ILD}).

AC Electrical Characteristics: See Section 2 for Test Methodology

Am i	lot = 16	V V	0.4			-40°C to +4			
Symbol	lor = 64	Par	rameter	V	cc = 3.3V ±			C = 2.7V	Units
	$V_j = 0.6$ $V_j = 2.0$	Au		Min	Typ (Note 1)	Max	Min	Bus-Held Input Max	(алони
t _{PLH}	S Propag	ation D	elay Data to Output	1.0	3.0	4.1 ^{9V} 4.1		Bus 0.2ld input Curro.3 to Char	ns (GO)tl
t _{PZH}	Output	Enable	Time	1.0 1.0	8.6 to 0	5.2 5.2	1.0 1.0	6.3 6.3	ns
t _{PHZ}	Output	Disable	Time	1.8 1.8	3.6	5.1 5.1	1.8 1.8	5.6 5.6	ns
toshl toshh	Output (Note 2		out Skew		3.6	1.0	ut Curren	Control Pin Inp	ns

Note 1: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacit	ance (Note 1)	lenoHel/IN				
Symbol	Parameter	Min	Тур	Max	Units	Conditions
CIN	Input Capacitance		4		pF	$V_{CC} = 0V, V_I = 0V \text{ or } V_{CC}$

 $V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC} Note 1: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012. nz, per mit-31D-0035, metrioù 301z.

pF

with TRI-STATE® Inputs/Outputs

General Description

ed applications. Gurrent sinking capability is 64 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A

These transceivers are designed for low-voltage (3.3V) Voc advanced BiCMOS technology to achieve high speed operation similar to 5V ABT white maintaining a low power dissi-

8

a Input and output interface capability to systems at 5V

Output Capacitance

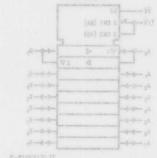
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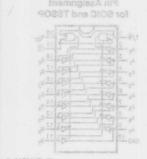
- It Bus-Hold data inputs eliminate the need for external
 - # Live insertion/extraction permitted
- it. Power Up/Down high impedance provides gitch-free
 - m Outputs source/sink -32 mA/+64 mA
 - M Available in SOIC JEDEC, SOIC EIAJ and TSSOP
 - ## Functionally compatible with the 74 series 245
 - M Latch-up performance exceeds 500 mA

Logic Symbols

Connection Diagram







Description
tput Enable Input ansmit/Receive Input
de A Inputs or TRI-STATE Outputs
te B Inputs or TRI-STATE Outputs

	OR	ASSET TRUE I			
Outputs	efugnt				
	買 VY				
Bus B Data to Bus A		1			
Bus A Data to Bus B		1			
HIGH-Z State	X	H			

TSSOP JEDEC	SOIC EIAJ	SOIC JEDEC	
74LVT245MTCX		74LVT245WM 74LVT245WMX	
		M20B	See NS Package Number

Pin Names

74LVT245

3.3V ABT Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

The LVT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

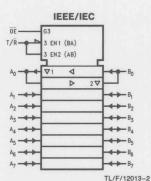
These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

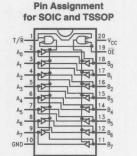
Features

- Input and output interface capability to systems at 5V VCC
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 245
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11 Logic Symbols

OE T/R B₀ B₁ B₂ B₃ B₄ B₅ B₆ B₇ TL/F/12013-1





TI /F/12013-3

Connection Diagram

Truth Table

Pin Names	Description
ŌĒ	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs
B ₀ -B ₇	Side B Inputs or TRI-STATE Outputs

Inputs		Outputs	
ŌĒ	T/R	Outputs	
L	L	Bus B Data to Bus A	
L	Н	Bus A Data to Bus B	
Н	X	HIGH-Z State	

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT245WM 74LVT245WMX	74LVT245SJ 74LVT245SJX	74LVT245MTCX
See NS Package Number	M20B	M20D	MTC20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})		-0.5V to +7.0V
DC Input Voltage (V _I)	PL 13	-0.5V to +7.0V
Output Voltage (V _O) Outputs in TRI-STATE	Ац	-0.5V to +7.0V
Outputs Active Value of Value	Aug	
DC Output Current (I _O) Output in LOW State Output in HIGH State, V _O > V _{CC}		01.0 128 mA 64 mA
DC Input Diode Current (I _{IK}) V _I < 0		-50 mA
DC Output Diode Current (IOK) VO < 0	0	-50 mA

Storage Temperature (T_{STG}) —65°C to +150°C Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating 100 20 Conditions

Supply Voltage Operating	2.7V to 3.6V
Input Voltage (V _I)	0V to 5.5V
Output Voltage (Vo)	
Output in Active State	OV to VCC
Output in "OFF" State	0V to 5.5V
Minimum Input Edge Rate (Δt/ΔV)	
$V_{IN} = 0.8V - 2.0V, V_{CC} = 3.0V$	document of 10 ns/V
Free Air Operating Temperature (T _A)	-40°C to +85°C

DC Electrical Characteristics

	n V _{CO} or GND.		Patiev TA = -	40°C to +85°C	enuo yliqque	Note 4: This is the increase in	
Symbol	Parameter (golobontol)	V _{CC}	Min Typ Max (Note 1)		Units	Conditions	
V _{IK}	Input Clamp Diode Voltage	2.7	Vcc	-1,2	V	$I_{\rm I} = -18 \rm mA$	
V _{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	V _O ≤ 0.1V or	
V _{IL}	Input LOW Voltage	2.7-3.6	8.8	0.8	munvasM	$V_0 \ge V_{CC} - 0.1V$	
VOH	Output HIGH Voltage	2.7-3.6	V _{CC} - 0.2	Jynamic Vol	muziniM	$I_{OH} = -100 \mu\text{A}$	
	(Note	2.7	2.4	namic Input Voltage	U Level I	$I_{OH} = -8 \text{ mA}$	
	etaVI) V	3.0	2.0	namic Input Veltage	V	$I_{OH} = -32 \text{mA}$	
V _{OL}	Output LOW Voltage	2.7	in tested.	0.2	V	$I_{OL} = 100 \mu\text{A}$	
КаніУ	g: 3V to threshold (V _{ILO}), 6V to threshold	2.7	nu-logni .Vč ai V0	grinding short t -0.5 ning	pute (V savi	I _{OL} = 24 mA	
		3.0		0.4	V	I _{OL} = 16 mA	
	VI.	3.0	507 101 3 110800	0.5	V	I _{OL} = 32 mA	
	C 10 + 88°C	3.0		0.55	V	I _{OL} = 64 mA	
I(HOLD)	Bus-Held Input Minimum Drive	3.0	75	eter	μΑ	V _I = 0.8V lodany3	
	4 272 304	3.0	-75		μΑ	V _I = 2.0V	
I(OD)	Bus-Held Input Over-Drive	3.0	500		μΑ	(Note 2)	
	Current to Change State	3.0	-5000.1	Data to Output	μΑ	(Note 3)	
l ₁	Input Current	0 or 3.6	1.0	10	μΑ	V _I = 5.5V JH9 [‡]	
an	Control Pins	3.6	1.1	±1 0/	μА	V _I = 0V or V _{CC}	
	Data Pins	3.6	0.1	-5	μΑ	V _I = 0V	
ns	5.9 2.2 6.5 4.8 2.0 4.8	3.0	2.2	1 90	μА	$V_I = V_{CC}$	
I _{IH} +	Control Pin Input Current	3.6		10	μΑ	V _{CC} ≤ V _I ≤ 5.5V	
OFF	Input or Output Current	0		±100	μΑ	$0V \le (V_1 \text{ or } V_0) \le 5.5$	

DC Electrical Characteristics (Continued)

	en	OHI	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		acciva mediana	If Military/Aerospece specified a	
Symbol	Parameter	V _{CC} (V)	Min	Typ (Note 1) Max	Units	Conditions (Conditions)	
lozL	TRI-STATE Output Leakage Current	3.6	Cuttout V	0.6pUo +7.6V	μΑ	DC Input Voltage (V) V0 = 0V	
lozh	TRI-STATE Output Leakage Current	3.6	Unitro	vos+ orten	μΑ	V _O = V _{CC} TATALIST of automO	
loz+	TRI-STATE Output Leakage Current	3.6	naseinikā	00V of Vi10 -	μΑ	V _{CC} ≤ V _O ≤ 5.5V evitoA atuqtuO	
ICCH	Power Supply Current = 55V V0.8 of 0.00 = (aT) entire comeT gold	3.6	V _{IN} = Free Air	Am 851 0.19	mA	$V_{I} = GND \text{ or } V_{CC},$ Outputs High	
ICCL	Power Supply Current	3.6		Am 08 – 12 Am 08 –	mA	V _I = GND or V _{CC} , Outputs Low	
Iccz	Power Supply Current	3.6		0.19	mA	V _I = GND or V _{CC} , outputs Disabled	
Icczn+	Power Supply Current	3.6		0.19	mA	$V_{I} = \text{GND or } V_{CC}, V_{CC} \le V_{O} \le 5.5V,$ Outputs Disabled	
ΔI _{CC}	Increase in Power Supply Current (Note 4)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	

Note 1: All typical values are at $V_{CC} = 3.3V$, $T_A = 25$ °C.

Note 2: An external driver must source at least the specified current to switch from LOW to HIGH.

Note 3: An external driver must sink at least the specified current to switch from HIGH to LOW.

Note 4: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Am 81 I Parameter	V _{CC} T _A = 25°C		Units	Conditions			
Syllibol	in V1.0 ≥ nV	(V)	Min	Тур	Max	Units	$C_L = 50 \text{ pF}, R_L = 500\Omega$	
VOLP	Quiet Output Maximum Dynamic VOL	3.3		0.8		V	(Note 2)	
VOLV A	Quiet Output Minimum Dynamic VOL	3.3	no.V	-0.8	-	V	(Note 2)	
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.7		V	(Note 3)	
VILD	Maximum Low Level Dynamic Input Voltage	3.3		nø.		V	(Note 3)	

Note 1: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 2: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output at LOW.

Note 3: Max number of data inputs (n) switching. n-1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}).

AC Electrical Characteristics: See Section 2 for Test Methodology

	l _{OL} = 64	V 88.0	$T_A = -40^{\circ}\text{C to } + 85^{\circ}\text{C}$ $C_L = 50 \text{ pF, R}_L = 500\Omega$					
Symbol	/8,0 = 1V Parameter /0.5 = 1V Au		Vcc	= 3.3V ±0.3V	eving m	V _{CC} =	V _{CC} = 2.7V	
			Тур					
	(Note 2)	Au	Min eoa	(Note 1)	Max	A-mMin	Max	
t _{PLH}	Propaga	tion Delay Data to Output	1.0008-		4.0	1.0	4.7	
t _{PHL}	V: = 5.51	Au 01	1.0	8.8 to 0	4.0	1.0	4.6	ns
tPZH ~~V	Output E	nable Time	1.1	3.6	5.5	no01.1	7.1	
tpzL	146 47		1.5		5.5	1.5	6.5	ns
PHZ	Output D	Pisable Time	2.2		5.9	2.2	6.5	
PLZ	00A = 1A		2.0		4.8	2.0	4.8	ns
OSHL	Output to	Output Skew		3.8	却	Input Curre	Control Pin	+
toslh ov K	(Note 2)				1.0	tout Curren	input or Ou	ns

Note 1: All typical values are at V_{CC} = 3.3V, T_A = 25°C.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

Capacitance (Note 1)

Symbol	Parameter	Min	Тур	Max	Units	Conditions
CIN	Input Capacitance		4		pF	$V_{CC} = 0V, V_I = 0V \text{ or } V_{CC}$
C _{I/O}	I/O Capacitance		8		pF	$V_{CC} = 3V$, $V_{I/O} = 0V$ or V_{CC}

Note 1: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

with TRI-STATE® Outputs

)escription |

The LVT373 consists of eight letches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is
HIGH. When LE is low, the data satisfying the input timing
requirements is latched, Data appears on the bus when the
Output Enable (OE) is LOW. When OE is HIGH, the bus
retrort is in the tinth impedance state.

has a cotal latches are designed for low-voltage (3.3V) $V_{\rm CO}$ applications, but with the capability to provide a TTL linear-

lace to a 5V environment. The LVT873 is fabricated with an

advanced BIOMOS technology to acrieve right speed operation similar to 5V ABT while mainteining a low power dissipation.

serures:

- is Input and output interhole capability to systems at 5V
- Bue-Hold data inputs eliminate the need for external outline resistors to hold unused incurs
 - I Live insertion/extraction permitted
- Power Up/Down high Impedance provides giltch-free bus leading
 - Cutputs source/sink -32 mA/+64 mA
 - s Available in SOIC JEDEC, SOIC EIAJ and TSSOP
 - # Functionally compatible with he 74 series 373
 - Am 002 sheavys accomposter murista Little

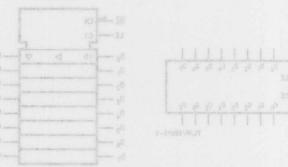
Ordering Codes see seemen

Locic Symbols

Connection Diagram







Latch Enable Input	
Output Enable Input	
TRI-STATE Latein Outputs	

TSSOP JEDEC	SOIC EIAJ	SOIC TEDEC	
74LVT373MTCX	74LVT373SJ 74LVT373SJX		

Semiconductor Street Band

74LVT373

3.3V ABT Octal Transparent Latch with TRI-STATE® Outputs

General Description

The LVT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

These octal latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

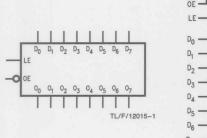
- Input and output interface capability to systems at 5V
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with he 74 series 373
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbols

Connection Diagram

Pin Assignment for



IEEE/IEC OE -0, 0, - 07

TL/F/12015-2

OE - 1	0	20
		20 - V _{CC}
00 - 2		19 - 07
D ₀ — 3		18 - D ₇
D ₁ - 4		17 - D ₆
0, - 5		16 - 06
02 - 6		15 - 05
D ₂ — 7		14 - D ₅
D ₃ — 8		13 - D ₄
03 — 9		12 - 04
GND - 10		11 - LE

Pin Names	Description			
D ₀ -D ₇	Data Inputs			
LE	Latch Enable Input			
ŌĒ	Output Enable Input			
00-07	TRI-STATE Latch Output			

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LVT373WM 74LVT373WMX	74LVT373SJ 74LVT373SJX	74LVT373MTCX
See NS Package Number	M20B	M20D	MTC20

standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

pull-up resistors to hold unused inputs

Live insertion/extraction permitted

Power Up/Down high impedance pro

	Inputs	Outputs	
LE	ŌĒ	Dn	On
X	Н	Х	ACCIZ/ INC
Н	L	L	Su e de se la man a
W HO!	-cu- C	SHOO	TECH VE.E
L	L	X	00

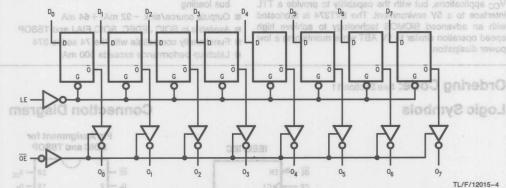
General Description

H = HIGH Voltage Level

X = Immaterial if the and should early on the second file of the control of the c

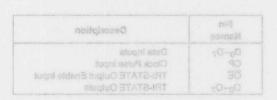
O₀ = Previous O₀ before HIGH to LOW transition of Latch Enable

Logic Diagram



16/1/160

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



		SOIC EIAJ	SOIC JEDEC	
X	74LVT374MTC	74LVT374SJ 74LVT374SJX	74LVT374WM 74LVT374WMX	
	MTC20	MZOD		See NS Package Number



LVT373 contains eight D-type latches with TRI-STATE ident outputs. When the Latch Enable (LE) input is

74LVT374 3.3V ABT Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The LVT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buff-ered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

These octal flip-flops are designed for low-voltage (3.3V) $V_{\rm CC}$ applications, but with the capability to provide a TTL interface to a 5V environment. The LVT374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

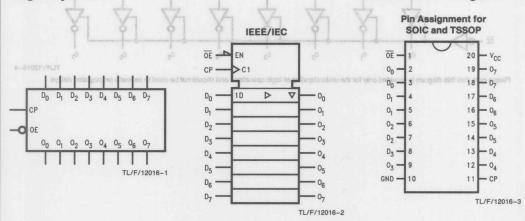
Features

- Input and output interface capability to systems at 5V Vccnt out and went purchased the entertail for second
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Functionally compatible with the 74 series 374
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbols

Connection Diagram



Pin Names	Description
D ₀ -D ₇	Data Inputs
CP	Clock Pulse Input
ŌĒ	TRI-STATE Output Enable Input
00-07	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number		74LVT374SJ 74LVT374SJX	74LVT374MTCX
See NS Package Number	M20B	M20D	MTC20

Functional Description

The LVT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time reguirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flipflops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

I Input and output interface capability to systems at 5V

a Bus-Hold data inputs eliminate the need for external

Live insertion/extraction permitted

Truth Table

	Outputs		
Dn	СР	ŌĒ	On
Н	5	L	4L VHT 646
Andrile	nations	· Lotan	TSAVE
X	Charles a s	10100	00
X		- H	E-19-17 PITTIN

or from the internal storage registers. Data on the A or B

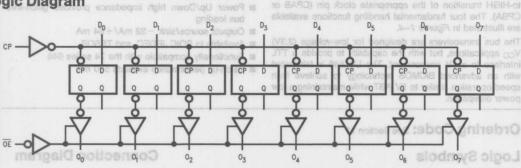
to-HIGH transition of the appropriate clock pin (CPAB or

LOGOHOLA ESC

General Description

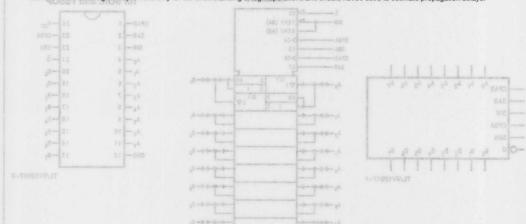
- H = HIGH Voltage Level
- L = LOW Voltage Level X = Immaterial
- A = immaterial
 Z = High Impedance
 Z = High Impedance
- = LOW-to-HIGH Transition bns agol-gift egyl-Q atuatuo niiw
- Oo = Previous Oo before HIGH to LOW of CP is a manual box ald from

Logic Diagram



TL/F/12016-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



YSSOP JEDEC		
	74LVT646WM 74LVT646WMX	Order Number
MTC24		See NS Package Number

Pin Names	Description
7A-0A	Data Register A Inputs
	Data Register A Outputs
	Data Register 8 Outputs
SAB, SBA	Transmit/Receive Inputs
0	Output Enable Input
	Direction Control Input

General Description

The LVT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figures 1–4*.

The bus transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

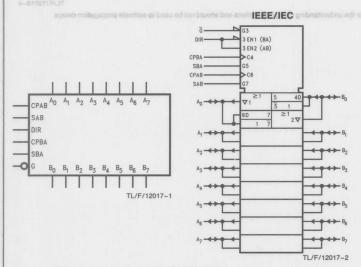
Features and affect the state of the flip floor and the

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused input
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC, and TSSOP
- Functionally compatible with the 74 series 646
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbols

Connection Diagram Pin Assignment

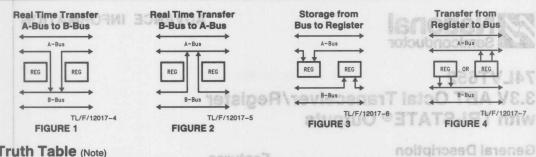


-v _{cc}	24	1	CPAB-
	23	2	SAB-
-SBA	22	3	DIR-
— <u>G</u>	21	4	A ₀ -
—В ₀	20	5	A1 -
—В ₁	19	6	A2-
-В2	18	7	A3 -
—В3	17	8	A ₄ -
-B ₄	16	9	A ₅ —
-B ₅	15	10	A ₆ —
—В6	14	11	A ₇ —
—B ₇	13	12	GND-

Pin Names	Description		
A ₀ -A ₇	Data Register A Inputs		
	Data Register A Outputs		
B ₀ -B ₇	Data Register B Inputs		
	Data Register B Outputs		
CPAB, CPBA	Clock Pulse Inputs		
SAB, SBA	Transmit/Receive Inputs		
G	Output Enable Input		
DIR	Direction Control Input		

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LVT646WM 74LVT646WMX	74LVT646MTCX
See NS Package Number	M24B	MTC24

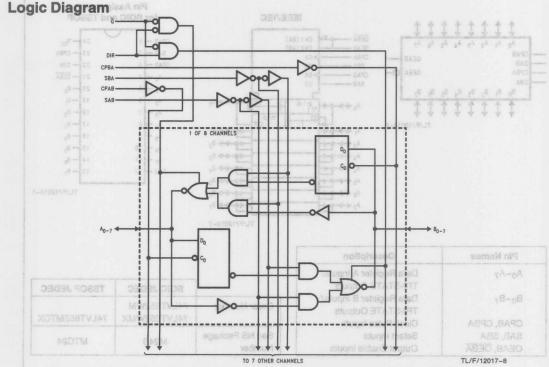
Logic Symbols



Truth Table (Note)

	Ve is ameleve Inputs sono ec		ametave Inputs and somethic function in the Data I/O				1/0	The LVT652 consists of bus transceiver circuits wi
G	DIR	CPAB	СРВА	SAB	SBA	A0-A7	B ₀ -B ₇	inp-nops, and controlled by ananged for ing
H H	X X X	H or L X	Hor L X	X X X	X X X	Input	Input O	Isolation Clock An Data into A Register Clock Bn Data into B Register
L L L	H H H	X HorL	X X AM X X TX	n 26 H 30 n 36 H 30 n 37 H 38	X X X	baoi aud an Input se ddeliavA se	Output	A _n to B _n —Real Time (Transparent Mode) Clock A _n Data into A Register A Register to B _n (Stored Mode) Clock A _n Data into A Register and Output to B _n
L L L	L L L	X X X	HorL	X X X	Pergama H H	Output	-nism eli Input	B _n to A _n —Real Time (Transparent Mode) Clock B _n Data into B Register B Register to A _n (Stored Mode) Clock B _n Data into B Register and Output to A _n

Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



(elon) SidsT dfunT

74LVT652

3.3V ABT Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The LVT652 consists of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

These bus/octal buffers and line drivers is/are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

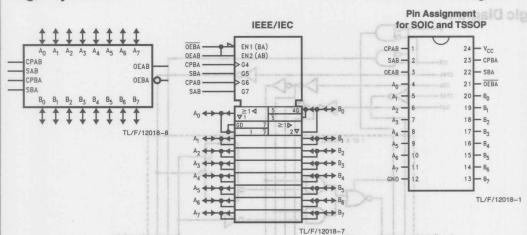
Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SOIC JEDEC and TSSOP
- Functionally compatible with the 74 series 652
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

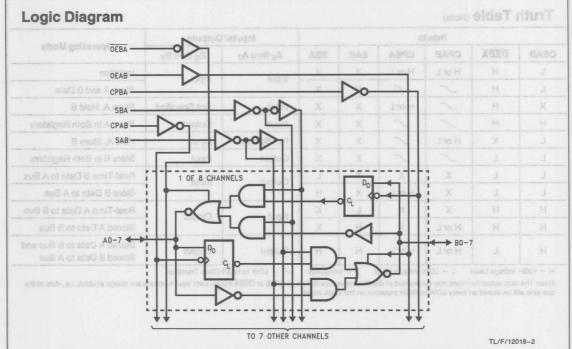
Logic Symbols

Connection Diagram



Pin Names	Description
A ₀ -A ₇	Data Register A Inputs/ TRI-STATE Outputs
B ₀ -B ₇	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
OEAB, OEBA	Output Enable Inputs

honomad	SOIC JEDEC	TSSOP JEDEC
Order Number	74LVT652WM 74LVT652WMX	74LVT652MTCX
See NS Package Number	M24B	MTC24



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

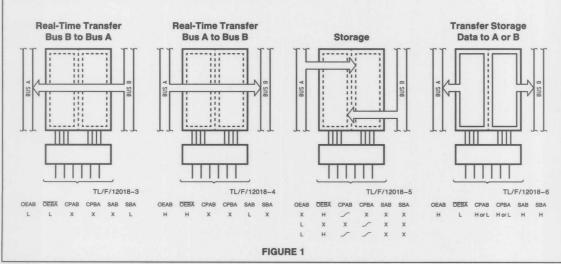
real-time.

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

priate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.



OEAB	OEBA	CPAB	СРВА	SAB	SBA	A ₀ thru A ₇	B ₀ thru B ₇	Operating Mode
L	Н	HorL	HorL	X	X	Input	Input	Isolation
L	Н	_	5	×	X	Input	Input	Store A and B Data
Χ	Н	_	HorL	X	X	Input	Not Specified	Store A, Hold B
Н	Н	_	~	Х	X	Input	Output	Store A in Both Registers
L	X	HorL	~	X	X	Not Specified	Input	Hold A, Store B
L	L	_	5	X	X	Output	Input	Store B in Both Registers
L	L	X	X	×	w ~ L	Output	Input	Real-Time B Data to A Bus
L	L	X	HorL	X	Н	Output	Input	Store B Data to A Bus
Н	Н	X	X	L	X	Input	Output	Real-Time A Data to B Bus
Н	Н	HorL	X	TH.	X		Output	Stored A Data to B Bus
Н	L	H or L	H or L	H	(H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

##

O 7 OTHER CHANNELS

-Brosever

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

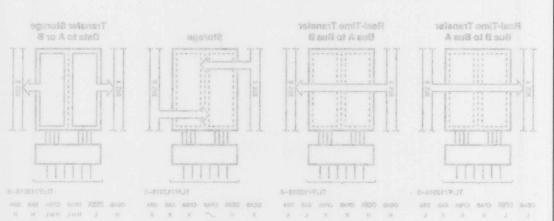
Functional Description

in the transceiver mode, data present at the HIGH Impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in Figure 7 demonstrate the four fundamental bus-management functions that can be performed with the LVTBSS.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appro-

or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEAB, in this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each sot of bus lines will remain at its last state.





74LVT16240 3.3V ABT 16-Bit Inverting Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled.

Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

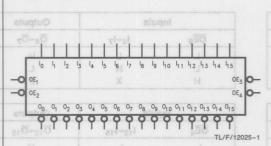
These buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



Pin Names	behavior deli = 3 Description	
OE _n	Output Enable Inputs (Active Low) Inputs	
$\overline{O}_0 - \overline{O}_{15}$	TRI-STATE Outputs	

	SSOP	TSSOP JEDEC
Order Number		74LVT16240MTD 74LVT16240MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

5				30
0E ₁ -	1	48	- OE ₂	
ō ₀ -	2	47	— I ₀	
ō ₁ -		46	— I ₁	Н
GND -	4	45	— GND	
ō ₂ -	5	44	-12	
ō ₃ -	6	43	-13	
V _{cc} -	7 F1 el	42	- V _{CC}	
ō ₄ -	8	41	-14	
ō ₅ -	9 14	40	- I ₅	1
GND -		39	— GND	
ō ₆ -	101=1	38	-16	
ō ₇ -		37	- I ₇	
ō ₈ -	13	36	- I ₈	
ō ₉ -	14	35	— I ₉	
GND -	15	34	- GND	
ō ₁₀ -	16	33	- I ₁₀	
ō ₁₁ -	17	32	- I _{1 1}	
v _{cc} -	18	31	- v _{cc}	
ō ₁₂ -	19	30	- I ₁₂	
ō ₁₃ -	20	29	-113	
GND -	21	28	— GND	
Ō ₁₄ -	22	27	- I ₁₄	
ō ₁₅ -	23	26	-I ₁₅	
OE ₄ -	24	25	$-\overline{OE}_3$	

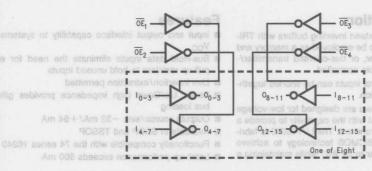
TL/F/12025-2

Functional Description

The LVT16240 contains sixteen inverting buffers with TRI-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The TRI-STATE out-

puts are controlled by an Output Enable (\overline{OE}_n) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Truth Tables

Inputs 27 bns 9022		SSC		Outputs	
OE ₁	_ [I ₀ -I ₃	ACTION ()		$\overline{O}_0 - \overline{O}_3$
L	30 - 01	L		Park	Н
L	47 10	Н	7		L
Н	1-197	X	6		Z

Inputs			3 3	Outputs
$\overline{\text{OE}}_3$	20V S	I ₈ -I ₁₁	The nov	0 ₈ -0 ₁₁
L	A	L	8 ,0	Н
L	el 0	Н	81-5	L
Н	010 83	V	01 - 000	Z

H = High Voltage Level L = Low Voltage Level

Inpu	Outputs	
OE ₂	14-17	$\overline{O}_4-\overline{O}_7$
		Н
art art artest ort or o	a d H e a	1 3 1 0 L
Н	X	Z 0-

Inputs		Outputs
OE ₄	I ₁₂ -I ₁₅	0 ₁₂ -0 ₁₅
L	L	Н
L	Н	L
Н	X	Z

X = Immaterial Z = High Impedance

 $\begin{array}{ccc} \overline{OE}_n & \text{Output Enable Inputs (Active} \\ & & & & & & & \\ \hline O_0 - \overline{O}_{16} & & & & & \\ \hline \end{array}$



TRI-STATE outputs. The device is nibble (4 bits) controlled with sent nibble that independent of the other. The control pins can be shorted together to obtain will 16 bits output the other.

74LVT16244
3.3V ABT 16-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

The LVT16244 contains sixteen non-inverting buffers with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

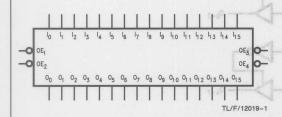
These bus buffers and line drivers are designed for low-voltage (3.3V) $V_{\rm CC}$ applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16244 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16244
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



	Pin Names	Description
ŌĒn	Output Enable Inputs (Active Low)	
	10-115	Inputs
	O ₀ -O ₁₅	Outputs

	SSOP	TSSOP JEDEC
Order Number		74LVT16244MTD 74LVT16244MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP

		-	
OE ₁ —	1	48	- OE ₂
00 -	2	47	- I ₀
0, -	3	46	-11
GND -	4	45	- GND
02 -	5	44	-12
03 —	6	43	-1 ₃
v _{cc} —	7	42	- v _{cc}
04 -	8	41	-14
05 -	9	40	-15
GND -	10	39	- GND
06 -	11	38	- I ₆
07 —	12	37	-17
08 -	13	36	- I ₈
09 -	14	35	— Ig
GND -	15	34	— GND
010-	16	33	-110
011-	17	32	- I _{1 1}
v _{cc} —	18	31	- v _{cc}
012	19	30	-112
013 -	20	29	-113
GND -	21	28	— GND
014	22	27	-114
015	23	26	-I ₁₅
OE ₄ —	24	25	$-\overline{OE}_3$

TL/F/12019-2

with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

1

Inputs OE ₁ I ₀ -I ₃		Outputs
		00-03
Ve to alrefeya of	villidease easheir	tugtuo bril tugni w
L	Н	H poV
eed for Hitemail	uts elimiXite the n	oni stab biZ-l-au8 a

and deliber	Inputs firmed neither	Outputs
OE ₃	I ₈ -I ₁₁	08-011
L	ink - 32 gnA/+64 mA	
L	90AST one 9	a Availahle in SSOI
s 19944	patible wix the 74 sede	m Functynally com

Connection Diagram
Pin Assignment for

H = High Voltage Level

L = Low Voltage Level

Inputs		Outputs
OE ₂	14-17	04-07
ettud phinavni-n	tontains Enteen no	AASSITV LOF
	ad of beHelceb stu	
		virb sserbiZ bru

012-015
12 915
ge (3.3V) Vo
ide H.

Ordering Code: See Section 11

X = Immaterial

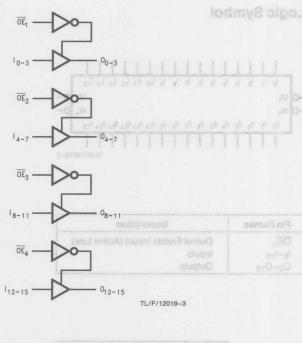
ABT 16-Bit Buffer/Line Driver

Z = High Impedance Q Wol

Logic Diagram

30 1-12

27 -14





Truth Tables

shugn!

The LVT16245 contains exteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte tunctioning identically, but independent of the other. The control pins can be shorted together

74LVT16245 3.3V ABT 16-Bit Transceiver with TRI-STATE® Outputs

Features

- Input and output interface capability to systems at 5V Vcc
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted level applied right = H
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16245
- Latch-up performance exceeds 500 mA

General Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $\overline{1/R}$ inputs determine the direction of data flow through the device. The $\overline{\text{OE}}$ inputs disable both the A and B ports by placing them in a high impedance state.

This non-inverting transceiver is designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16245 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Ordering Code: See Section 11

Logic Symbol



Pin Names	Description
ŌĒn	Output Enable Input (Active Low)
T/Rn	Transmit/Receive Input
A ₀ -A ₁₅	Side A Inputs/TRI-STATE Outputs
B ₀ -B ₁₅	Side B Inputs/TRI-STATE Outputs

	SSOP	TSSOP JEDEC
Order Number	74LVT16245MEA 74LVT16245MEAX	74LVT16245MTD 74LVT16245MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP



TL/F/12020-2

Functional Description

The LVT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.



Truth Tables

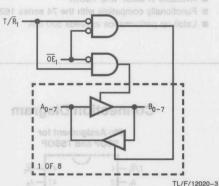
Inputs		Outputs	
OE ₁	T/R ₁	Features	
a is emo	iny 19 syste	Bus B ₀ -B ₇ Data to Bus A ₀ -A ₇	
L	н	Bus A ₀ -A ₇ Data to Bus B ₀ -B ₇	
Н	X	HIGH-Z State on A ₀ -A ₇ , B ₀ -B ₇	

H = High Voltage Level

Inj	outs	Outputs	
OE ₂	T/R ₂	General Description	
derible on	meval non	Bus B ₈ -B ₁₅ Data to Bus A ₈ -A ₁₅	
Loop	Н	Bus A ₈ -A ₁₅ Data to Bus B ₈ -B ₁₅	
Н	X	HIGH-Z State on A ₈ -A ₁₅ , B ₈ -B ₁₅	

X = Immaterial Z = High Impedance Z = High Impedance

Logic Diagrams SE- antellecture attique at



1 0F 8 20MOIS 5 TL/F/12020-4

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Side A Inputs/TRI-STATE Outputs	
Side B Inputs/TRI-STATE Outputs	B ₀ -B ₁₅

74LVT16373 3.3V ABT 16-Bit Transparent Latch leading in the strong of t

General Description

The LVT16373 contains sixteen non-inverting latches with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the outputs are in high Z state.

These latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16373 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features in O of no tresent sew that nothermolni

- Input and output interface capability to systems at 5V VCC
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16373
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Logic Symbol



TL/F/12021-1

Pin Names	Description
OE _n	Output Enable Input (Active Low) Latch Enable Input
I ₀ -I ₁₅ O ₀ -O ₁₅	Inputs TRI-STATE Outputs

TUE	SSOP	TSSOP JEDEC
Order Number	74LVT16373MEA 74LVT16373MEAX	74LVT16373MTD 74LVT16373MTDX
See NS Package Number	MS48A	MTD48

Connection Diagram

Pin Assignment for SSOP and TSSOP

- 3		/	
OE ₁ —	1/1	48	- LE ₁
00 -	2	47	-1 ₀
01-	3	46	— I ₁
SND —	40	45	- GND
02 -	5	44	- I ₂
03 —	6	43	— I ₃
v _{cc} —	7	42	- v _{cc}
04-	8	41	-14
05 -	9	40	-15
ND -	10	39	- GND
06-	11	38	-16
07 -	40	37	-17
08-	13	36	-18
09 -	14	35	- l ₉
ND -	15	34	- GND
010 -	16	33	-40
0,1	17	32	-111
v _{cc} —	1.8	31	- v _{cc}
012 —	19	30	- I _{1 2}
013	20	29	-113
ND —	21	28	- GND
014 —	22	27	-114
015	23	26	-I ₁₅
DE ₂ —	24	25	-LE ₂

TL/F/12021-2

16-bit operation. The following description applies to each byte. When the Latch Enable (LEn) input is HIGH, data on the D_n enters the latches. In this condition the latches are transparent, i.e., a latch output will change states each time its D input changes. When LEn is LOW, the latches store information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LEn. The TRI-STATE standard outputs are controlled by the Output Enable $(\overline{\text{OE}}_n)$ input. When $\overline{\text{OE}}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{\text{OE}}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

■ Outputs source/sink -32 mA/+64 mA

M Latch-up performance exceeds 500 mA

1	X	Н	EXX	Z	
2 0	randba	y Lang	Lar trad	Volo	
	troa House and a	1 716	H	H	
	tudino.	O L	X	Oo	

Inputs 19399 H			Outputs
LE ₂	OE ₂	I ₈ -I ₁₅	08-015
ne fluXlops	Contil Hed. T	a devicX is byte	ciZions. Th
(B. Helden	en the Latch E	to the data whe	Iransparent
the Hrup	a that meets	s lovi, Hhe dath	VHon LE
the Optput	nariw gud erli	no engage et	oned. De

These latches are designed for low

H = High Voltage Level

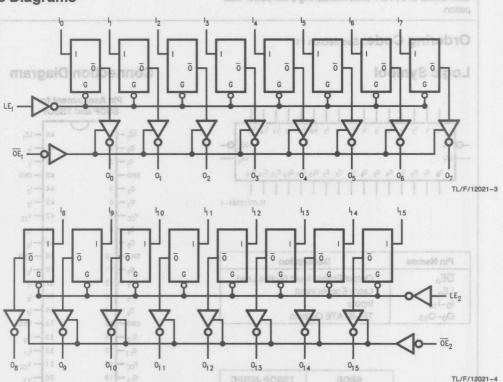
L = Low Voltage Level

X = Immaterial

plications, but with the capability to expendent all = Zertace

Oo = Previous output prior to HIGH to LOW transition of LE

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.



74LVT16374 3.3V ABT 16-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The LVT16374 contains sixteen non-inverting D flip-flops with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

These flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

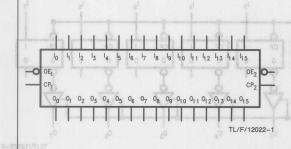
Features

- Input and output interface capability to systems at 5V
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs and Holden
- Live insertion/extraction permitted gnl =30 and to not
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

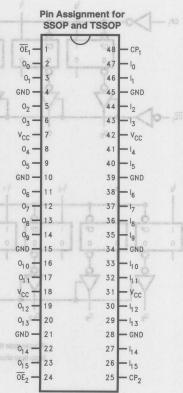
Logic Symbol

Connection Diagram



Pin Names	Description
ŌĒn	TRI-STATE Output Enable Input (Active Low)
CPn	Clock Pulse Input
10-115	Data Inputs
00-015	TRI-STATE Outputs

O1S	SSOP	TSSOP JEDEC	
Order Number	74LVT16374MEA 74LVT16374MEAX	74LVT16374MTD 74LVT16374MTDX	
See NS Package Number	MS48A	MTD48	



TL/F/12022-2

Functional Description

The LVT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CPn) transition. With the Output Enable $(\overline{\text{OE}}_n)$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{\text{OE}}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

■ Outputs source/sink -32 mA/+64 mA

■ Latch-up performance exceeds 500 mA

Eurotionally compatible with the 74 series 16374

W Available in SSOP and TSSOP

Truth Tables

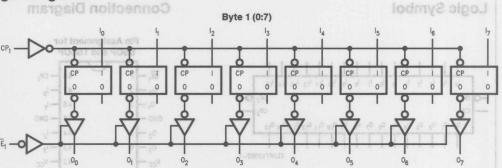
	Inputs	mooims	Outputs
CP ₁	OE ₁	I ₀ -I ₇	00-07
_	L	HOL	H
1	a muin	or bro	a secto
J.C. Sin.	a minda	X	00
X	Н	X	Z

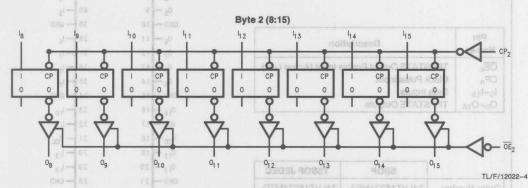
renting D file	874 contains sixteen inventing D					
CP ₂ A	OE ₂ and a	18-I ₁₅	08-015			
/	OE) are common or full 15-bit on	H	H			
	flov-wal not ber	L	These flip-fl			
The state of the s		X with the ca	00			
he X	a LVTINETA is	X	ma Va Zot			

TL/F/12022-3

- -1900 H = High Voltage Level of veolonitosi SOMOIS beonsybs
- lasib La Low Voltage Level main silder TSA V3 of ralimia notice
 - X = Immaterial
 - Z = High Impedance
 - Oo = Previous Oo before HIGH to LOW of CP

Logic Diagrams





Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.



74LVT16646 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE® Outputs

General Description

The LVT16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

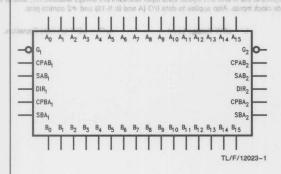
Features

- Input and output interface capability to systems at 5V VCC
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11 Logic Symbol

Connection Diagram

Pin Assignment for SSOP and TSSOP



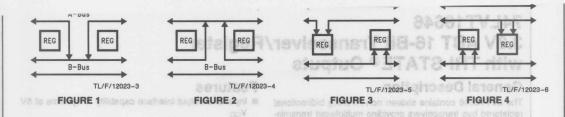
	SSOP	TSSOP JEDEC
Order Number	74LVT16646MEA 74LVT16646MEAX	74LVT16646MTD 74LVT16646MTDX
See NS Package Number	MS56A	MTD56

SSOP and TSSOP							
anest His			io besota ed lii				
DIR ₁	1	56	— G ₁				
CPAB -	2	55	- CPBA ₁				
SAB ₁ -	3	54	- SBA ₁				
GND -	4	53	- GND				
A ₀ —	5	52	— B ₀				
A1 -	6	51	— B ₁				
v _{cc} —	7	50	- v _{cc}				
A ₂ —	8	49	— в ₂				
A3 -	9	48	— B ₃				
A ₄ —	10	47	— B ₄				
GND -	11	46	- GND				
A ₅ —	12	45	— B ₅				
A ₆ —	13	44	— B ₆				
A7 -	14	43	— В ₇				
A ₈ —	15	42	— B ₈				
A9 -	16	41	— В9				
A10 -	17	40	— B ₁₀				
GND -	18	39	— GND				
A11 -	19	38	— B _{1 1}				
A12 -	20	37	- B ₁₂				
A13-	21	36	— B ₁₃				
v _{cc} —	22	35	- v _{cc}				
	23	34	- B ₁₄				
A15-	24	33	-B ₁₅				
GND -	25	32	— GND				
SAB ₂ -	26	31	- SBA ₂				
CPAB ₂	27	30	- CPBA ₂				
DIR ₂	28	29	$-\bar{G}_2$				

TL/F/12023-2

Note: The

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.



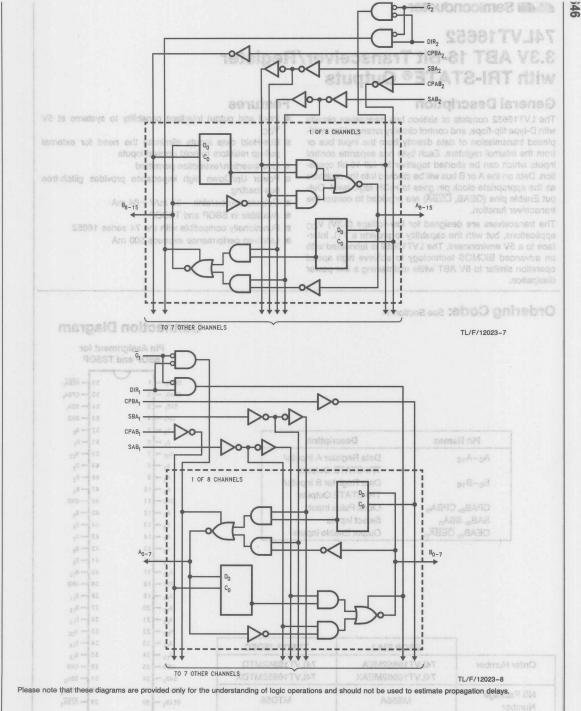
Bus-Hold data inputs elimin

Truth Table (Note)

	Live insertion/extraction applied						a I/O	Output Operation Mode
G ₁	DIR ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA ₁	A ₀₋₇	B ₀₋₇	device. The CPAB and CPBA inputs load of
Н	×	HorL	H or L	X	X	Input	Input	Isolation Clock An Data into A Register
Н	04 X 1 8	ne 7X series	r dhy z nátn	anox vitar	F.Xedor	this to	riske the start and a	Clock Bn Data Into B Register
L	Н	X	X	annothed o	X	beads	rigirt avea	An to Bn—Real Time (Transparent Mode)
L	Н	_	X	L	X	Input	Output	Clock An Data to A Register
L	Н	HorL	X	Н	X		Output	A Register to Bn (Stored Mode)
L	Н	5	X	Н	X	and the state of t		Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An-Real Time (Transparent Mode)
L	L	X	1	X	L	0.44	Immut	Clock Bn Data into B Register
L	L 888	X	HorL	X	Н	Output	Input	B Register to An (Stored Mode)
L	L	X	mip La net	X	Н			Clock Bn into B Register and Output to An

Note: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

H = HIGH Voltage Level _ = LOW-to-HIGH Transition. X = Immaterial L = LOW Voltage Level CPARA - 22 Proliminary Data: Harlonel Semiconductor reserves the right to make changes at any time without notice.





74LVT16652 3.3V ABT 16-Bit Transceiver/Register with TRI-STATE® Outputs

General Description

The LVT16652 consists of sixteen bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Each byte has separate control inputs which can be shorted together for full-16-bit operation. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBĀ) are provided to control the transceiver function.

The transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16652 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Available in SSOP and TSSOP
- Functionally compatible with the 74 series 16652
- Latch-up performance exceeds 500 mA

Ordering Code: See Section 11

Connection Diagram

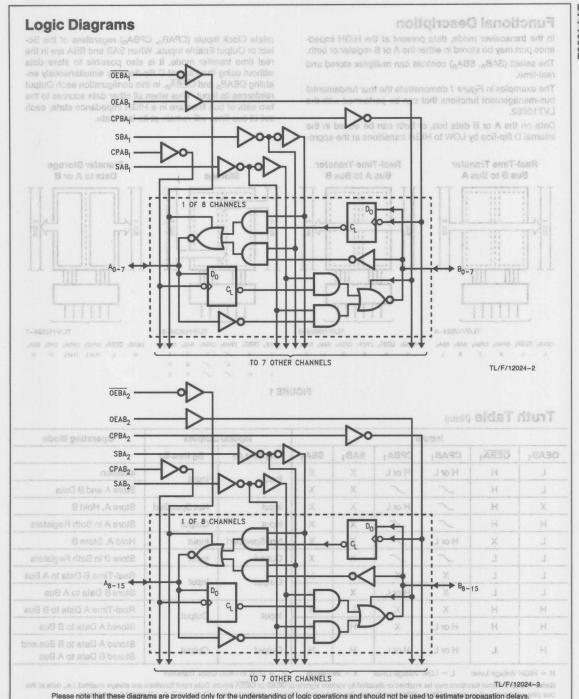
Pin Assignment for SSOP and TSSOP



Pin Names	Description
A ₀ -A ₁₆	Data Register A Inputs/
29.0	TRI-STATE Outputs
B ₀ -B ₁₆	Data Register B Inputs/
	TRI-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
SAB _n , SBA _n	Select Inputs
OEAB _n , OEBA _n	Output Enable Inputs

	SSOP EIAJ	TSSOP JEDEC
Order Number	74LVT16652MEA	74LVT16652MTD
8-698619141	74LVT16652MEAX	74LVT16652MTDX
NS Package Number	MS56A	MTD56

TL/F/12024-1



ב ... ביוויסי עוס א טו בי ופקומנפו טו שטנוו. The select (SABn, SBAn) controls can multiplex stored and real-time.

The examples in Figure 1 demonstrate the four fundamental bus-management functions that can be performed with the LVT16652.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the approject or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB_n and OEBA_n. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

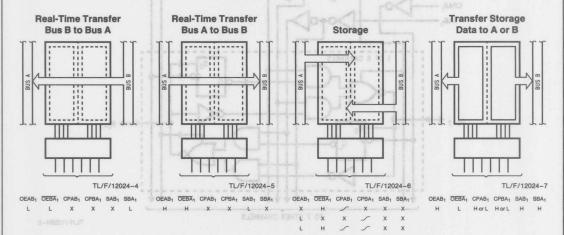


FIGURE 1

Truth Table (Note)

		Inpu	ts	-0<		Inputs/	Outputs	Operating Mode
OEAB ₁	OEBA ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA ₁	A ₀ thru A ₇	B ₀ thru B ₇	- 58A2
L	Н	H or L	HorL	X	X	Input	Input	Isolation
L	Н	5	1	X	X	Input	Impat	Store A and B Data
X	Н	_	HorL	X	X	Input	Not Specified	Store A, Hold B
Н	Н	_	1	X	X	Input 2JIRRA	Output	Store A in Both Registers
L	Х	H or L	150	X	X	Not Specified	Input	Hold A, Store B
L	L	1	5	×	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L (8)	X	HorL	X	н	Output	all light	Store B Data to A Bus
Н	Н	Х	X	L	X	Input	Output	Real-Time A Data to B Bus
Н	Н	H or L	X	H	X	- P	Output	Stored A Data to B Bus
Н	L	H or L	HorL	н	Н	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Note: The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs. This also applies to data I/O (A and B: 8-15) and #2 control pins.

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Bookshelf	
Distributors no lane mid leadey 19	





Ordering Information Office of the Package Offering Total Package Offering

Low Voltage Logic Ordering Information

Available and Planned Package Offering

For most current packaging information, contact your National Semiconductor representative.

Туре	Lead Count	LVQ	LVX	LCX	defined as follows:
00	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
02	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	Family	Temperature Range
04	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	Contract Con	74 = Commercial
08	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		
14	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		Device Type
32	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP		Package Code
74	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	rall Outline Package, JEDEC	S = Molded Sn
86	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	de) Molded Small Outline P	
125	14	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	all Outline Package, JEDEC	SOIC JEDEC & EIAJ, TSSOF
138	16	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	n as QSOP)	wonxi calab know
151	16	SOIC JEDEC & EIAJ			
157	16	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	The second of the Van or Sun of the	- Carles - T VIII-1
174	16	SOIC JEDEC & EIAJ	SOIC JEDEC & EIAJ, SSOP I, TSSOP	dering Informatio	TAY LSIMBA OL
240	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOI
241	20	SOIC JEDEC & EIAJ, QSOP			defined as follows:
244	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOI
245	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOI
273	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	e Range Family	Temperatu
373	20 10	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOI
374	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	SOIC JEDEC & EIAJ, TSSOP	SOIC JEDEC & EIAJ, TSSOI
573	20	SOIC JEDEC & EIAJ, QSOP	SOIC JEDEC & EIAJ, SSOP I, TSSOP	0	Device Typ
646	24			SOIC JEDEC, TSSOP	SOIC JEDEC, TSSOP
652	24		age, JEDEC	SOIC JEDEC, TSSOP	SOIC JEDEC, TSSOP
3245	24		SOIC JEDEC, QSOP LAIE, SOE	Molded Small Outline Pack	= 18
4245	24		SOIC JEDEC, QSOP GOVT LAIR . OG	Shrink Smell Outline Packa	= DSM
C3245	24		SOIC JEDEC, QSOP		
C4245	24		SOIC JEDEC, QSOP		
3L383	24		SOIC JEDEC, QSOP	Family Ordering	LVX Translato
3L384	2497	tokage type and temperat	SOIC JEDEC, QSOP miss flotted ball	sed to form part of a simpl	The device number is u
16240	48			SSOP, TSSOP	SSOP, TSSOP
16244	48			SSOP, TSSOP	SSOP, TSSOP
16245	48		VX C XXXX WM X	SSOP, TSSOP	SSOP, TSSOP
16373	48	enotial Variations	.0	SSOP, TSSOP	SSOP, TSSOP
16374	48	scial variagons X" = Tape and Reel		SSOP, TSSOP	SSOP, TSSOP
16646	56	" = Rail/Tube		SSOP, TSSOP	SSOP, TSSOP
16652	56	Sur that		SSOP, TSSOP	SSOP, TSSOP

Ordering Information and Physical Dimensions

Low Voltage Logic Ordering Information

LVQ Family Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

Temperature Range Family
74 = Commercial

Device Type

Package Code
S = Molded Small Outline Package, JEDEC

74LVQ XXX S C X
Special Variations
"X" = Tape and Reel
" " = Rail/Tube

Temperature Range
C = Commercial (-40°C to +85°C)

SJ = (0.300" Wide) Molded Small Outline Package, EIAJ

QS = Shrink Small Outline Package, JEDEC
(also known as QSOP)

LVX Family Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

Temperature Range Family

74 = Commercial

Device Type

Package Code

M = Molded Small Outline Package, JEDEC

SJ = Molded Small Outline Package, EIAJ

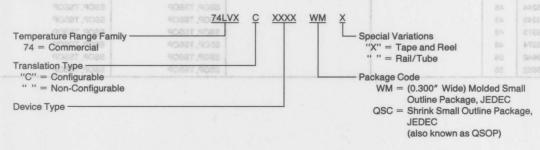
MSC = Shrink Small Outline Package, EIAJ, Type I

Special Variations
"X" = Tape and Reel
"" = Rail/Tube

Available and Planned Package Offering

LVX Translator Family Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



68-Le			20-Load	bes.l-81	beed-							
		BASM	BOSM	MISA	74	LVX3L	XXX	WN	<u>/</u>	sall Outline		
	Temperatu		BUSIM	AOTM	Apik		DECE	age,	Paci		al Variations	M
	74 = Co	mmercial	M20B	Banw		4	38081	uge,		onibua"	Tape and ReRail/Tube	MW
	Family -	Bus Swi	tehee	M16D	#14D	1		-			Molded Sm	
	Device Typ		MSC20	MSG18	#roa	M	,egs.k	na Pac				
	Package C		Vide) Molde	ed Small Ou	tline Pac	kane IFI	DEC					
				Package, J			as QS	SOP)			JEDEC, 4,4	
			OSAOM								Molded Shr JEDEC (als	
MSSS	A8ASM-											
	amily C		land the same of t								DEDEC	
	s follows:	s used to	form part o	of a simplifie	ed purch	asing coo	ie whe			and the same of	and temperatu	ire range ar
						74LCX	XXX	М	X			
	Temperat	ure Range	Family —				T	T	L	- Special \	/ariations	
		ommercia	1 108	ompari	ge C		eni	BUC		"X" =	Tape and Re	EDECI
	Device Ty	rpe ——									Rail/Tube	
MD88		-			analist .						Elina .	Paoliage
	Package (Wide) Mold	ed Small O	utline Pa	ckage, JE	DEC	100000				
	WM =	= (0.300"	Wide) Mold	ed Small O	utline Pa	ckage, JE	DEC	0.245				
				ed Small O								
	(7.40)		Body Width		age, occ	(08.8)					8	
				Package,			ad)			0.295		
	MTD =		rink Small C Body Width	utline Pack	age, JEL	(S8.V)		(01.8)				
	1	813								0.205		
										(5.20)		
VTE	omily (Judovin			38.0					0.240		
	amily C		202					(6.70)			and townsort	9088
	s follows:	s used to		The state of the s	ea purcr	asing cod		re the		kage type	and temperatu	ire range ar
						74LVT	xxx	OM.	x			
	(6.20)	(08.	8) (0			(08.8)		(08.80)		(08.8) Cassiel	(ariations	
0.177		ture Range		0.16	0.177	0.169		0.177			/ariations Tape and Ree	
(4.50)					(4.50)	(4.30)		(4,50)			Rail/Tube	
	Device Ty	241	.0	08.0								
	Package		wido) Mold	od Small O	utlino Po	ckago IE	DEC					
				ed Small Or led Small Or								
	SJ :	= (0.300"	Wide) Mold	ded Small O	utline Pa	ackage, El						
	MEA :	4.4 mm = Shrink S = Thin Sh	Body Width Small Outlin	e Package, Outline Pack	JEDEC	(48/56-Le	ad)	m_				

ens MTD and

Package Code	Description	NS Package Number								
Package Code	Description	14-Lead	16-Lead	20-Lead	24-Lead	48-Lead	56-Lead			
S	Molded Small Outline Package, JEDEC	M14A	M16A	M20B	M24B					
М	Molded Small Outline Package, JEDEC	M14A	M16A	M20B	M24B	Temperal				
WM	Molded Small Outline Package, JEDEC	M14B	M16B	M20B	M24B	74 - 0				
SJ	Molded Small Outline Package, EIAJ	M14D	M16D	M20D	we aug =	Family —				
MSC	Molded Shrink Small Outline Package, EIAJ, Type I	MSC14	MSC16	MSC20	əq	Device Ty				
MTC	Molded Thin Shrink Small Outline Package, JEDEC, 4.4 mm Body Width	MTC14	MTC16	MTC20	MTC24	Package WW				
QS	Molded Shrink Small Outline Package, JEDEC (also known as QSOP)	(0915) 020	ic joganos	MQA20	MQA24					
MEA	Molded Shrink Small Outline Package, JEDEC	1	matio	ng Info	Orderia	MS48A	MS56A			

MTD48

MTD56

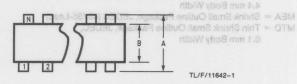
JEDEC-EIAJ-SSOP Small Outline Package Comparison

Molded Thin Shrink Small Outline Package,

JEDEC, 6.1 mm Body Width

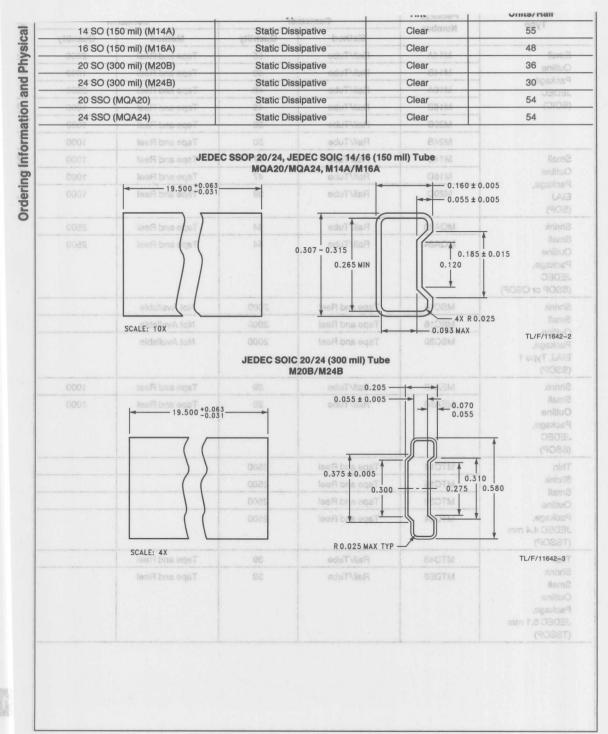
Dookogo	Dim	14-	-Pin	16	-Pin	20	-Pin	gyTeolve24	-Pin
Package	Dilli	Min	Max	Min	Max	Min	Max eh	PacniMe Co	Max
SOIC	А	0.228 (5.80)	0.245 (6.20)	0.228 (5.80)	0.245 (6.20)	0.393 (10.0)	0.420 (10.65)	0.393 (10.0)	0.420 (10.65
JEDEC	В	0.149 (3.80)	0.158 (4.00)	0.149 (3.80)	0.158 (4.00)	0.291 (7.40)	0.300 (7.60)	0.291 (7.40)	0.300 (7.60)
SOIC	А	0.295 (7.50)	0.319 (8.10)	0.295 (7.62)	0.319 (8.89)	0.295 (7.62)	0.319 (8.89)	= CITM	
EIAJ	В	0.205 (5.20)	0.213 (5.40)	0.205 (5.20)	0.213 (5.40)	0.205 (5.20)	0.213 (5.40)		
SSOP Type I	A	0.240 (6.10)	0.264 (6.70)	0.240 (6.10)	0.264 (6.70)	0.240 (6.10)	0.264 (6.70)	amily Or	LVT F
	В	0.165 (4.20)	0.181 (4.60)	0.165 (4.20)	0.181 (4.60)	0.165 (4.20)	0.181 (4.60)	follows:	es banilei
TSSOP	A	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)	0.244 (6.20)	0.260 (6.60)
TSSOP	Tapegind Fi Rail/Tuba	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)	0.169 (4.30)	0.177 (4.50)
SSOP	А				0 11 0	0.231 (5.87)	0.241 (6.12)	0.231 (5.87)	0.241 (6.12)
aka QSOP)	В			kage, JEDED kage, JEDED Skage, EIAJ		0.151 (3.84)	0.157	0.151 (3.84)	0.157

Units: Inch (mm)



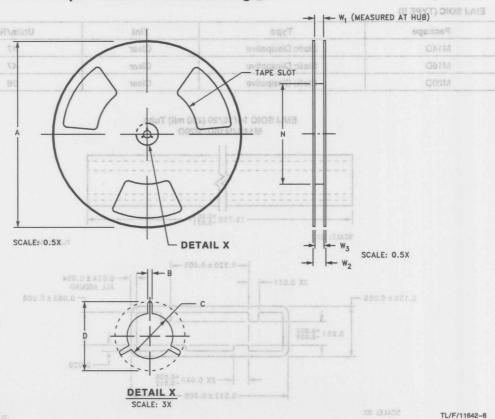
MTC = Thin Shrink Small Outline Package, JEDEC.

Package	NS Package Number	Primar Immedia Contain	ite	Seconda Immedia Contain	9
.88	Number	Method	Quantity	Method	Quantity
Small	M14A	Rail/Tube	55	Tape and Reel	2500
Outline 88	M14B	Rail/Tube	50	Tape and Reel	1000
Package, JEDEC	M16A	Rail/Tube	48	Tape and Reel	2500
(SOIC)	M16B	Rail/Tube	25 45	Tape and Reel	1000
54	M20B	Rail/Tube	36	Tape and Reel	1000
	M24B	Rail/Tube	30	Tape and Reel	1000
Small	M14D	Rail/Tube	SSOP(4) 24, JE	Tape and Reel	1000
Outline	M16D	Rail/Tube	47	Tape and Reel	1000
Package, 2003 EIAJ 2003 (SOP)	M20D	Rail/Tube	38	Tape and Reel	1000
Shrink	MQA20	Rail/Tube	54	Tape and Reel	2500
Small Outline 210.0 x Package, JEDEC (SSOP or QSOP)	MQA24 881.0 0S1.0	Rail/Tube - vos.	54	Tape and Reel	2500
Shrink	MSC14	Tape and Reel	2000	Not Available	
Small 850	MSC16	Tape and Reel	2000	Not Available	
Outline Package, EIAJ, Type 1 (SSOP)	MSC20	Tape and Reel aduT (6m 000) AS\08 EASRA\600	2000 JEDEC SOIC M	Not Available	
Shrink	MEA48	- 809 Rail/Tube	29	Tape and Reel	1000
Small Outline Package, JEDEC (SSOP)	ore MEA56	Rail/Tube	29	Tape and Reel	1000
Thin	MTC14	Tape and Reel	2500		
Shrink 086.0	MTC16	Tape and Reel	2500		
Outline	MTC20	Tape and Reel	2500		
Package, JEDEC 4.4 mm (TSSOP)	MTG24	Tape and Reel	2500		
Thinsantaur	MTD48	Rail/Tube	39	Tape and Reel	
Shrink Small Outline Package, JEDEC 6.1 mm	MTD56	Rail/Tube	39	Tape and Reel	



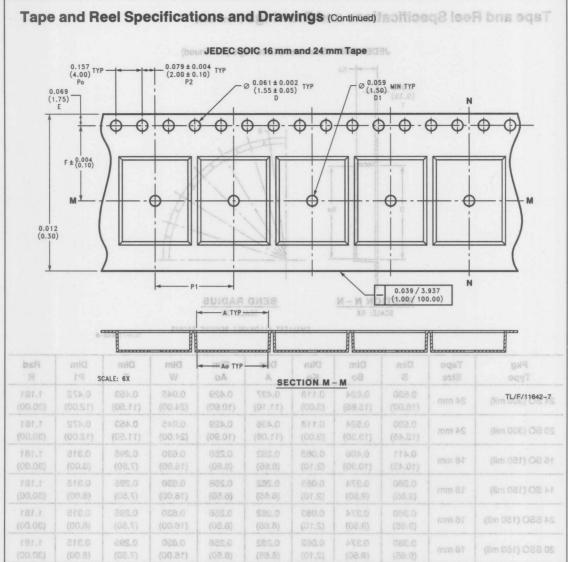
Package		Туре	-1-		Tint		Jnits/Rail	
M14D	-	Static Dissipative		Clear			47	
M16D		Static Dissipative	1	Clear			47	
M20D		Static Dissipative	W	1	Clear	\	38	
	2CALE: 0.	SCALE: 8X	9.750 +0.063 9.750 +0.063 9.750 ±0.003		0.024 ± 0.0 ALL AROUN	D 0.083 ± 0.0		
	CALF. 8Y	→	2X 0.0					
3-24011/3\/IT	SCALE: 8X	s and 24 mm Tape	-0.512 ± 0.00	8 <u>X 318</u> 8	SCAL		TL/F/	11642–5
2 11./F/11042-8 Wg	CALE: 8X	e and 24 nm Tage	-0.512 ± 0.00	8 <u>X 318</u> 8	SCAL		TL/F/	
9-3901(1).11			-0.512 ± 0.00	E 3x 80	JASE Meal9	0.058		11642-5 equi 9218

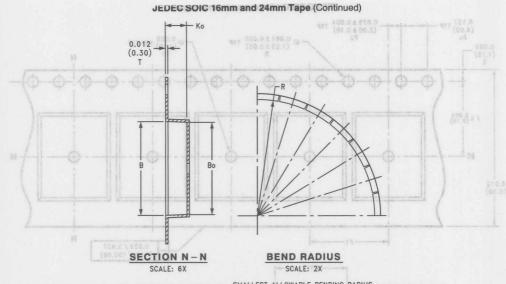




Plastic 13" Reel for 16 mm and 24 mm Tape

Tape Size	A	В	С	D	N	W ₁	W ₂	W ₃
24 mm	13.00	0.059	0.512 ± 0.008	0.795	7.000	0.961 + 0.078/-0.000	1.197	W ₁ +0.078/-0.039
	330.0	1.50	13.00 ± 0.20	20.20	178.00	24.40 +2.00/-0.00	30.40	W ₁ +2.00/-1.00
16 mm	13.00	0.059	0.512 ± 0.008	0.795	7.000	0.646 + 0.078/-0.000	0.882	W ₁ +0.078/-0.039
	330.0	1.50	13.00 ± 0.20	20.20	178.00	16.40 +2.00/-0.00	22.40	W ₁ +2.00/-1.00

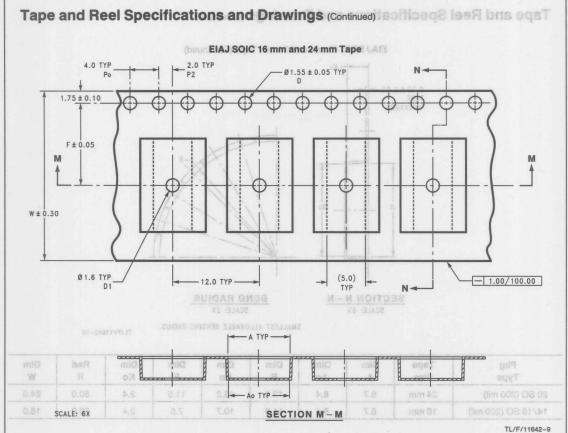




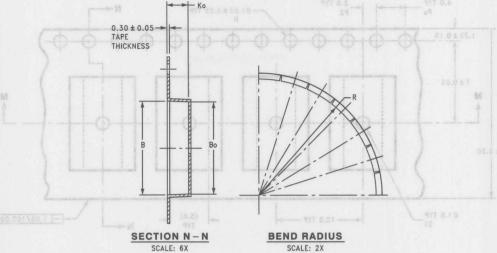
SMALLEST ALLOWABLE BENDING RADIUS.

TL/F/11642-8

Pkg Type	Tape Size	Dim B	Dim Bo	Dim Ko	Dim A	Dim Ao	Dim W	Dim Frank	Dim P1	Rad R
24 SO (300 mil)	24 mm	0.630 (16.00)	0.624 (15.85)	0.118 (3.00)	0.437 (11.10)	0.429 (10.90)	0.945 (24.00)	0.453 (11.50)	0.472 (12.00)	1.181
20 SO (300 mil)	24 mm	0.530 (13.45)	0.524 (13.30)	0.118 (3.00)	0.436 (11.08)	0.429 (10.90)	0.945 (24.00)	0.453 (11.50)	0.472 (12.00)	1.181
16 SO (150 mil)	16 mm	0.411 (10.45)	0.406 (10.30)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181
14 SO (150 mil)	16 mm	0.380 (9.65)	0.374 (9.50)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181
24 SSO (150 mil)	16 mm	0.380 (9.65)	0.374 (9.50)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181
20 SSO (150 mil)	16 mm	0.380 (9.65)	0.374 (9.50)	0.083 (2.10)	0.262 (6.65)	0.256 (6.50)	0.630 (16.00)	0.295 (7.50)	0.315 (8.00)	1.181



Tape and Reel Specifications and Drawings (Continued) EIAJ SOIC 16 mm and 24 mm Tape (Continued)



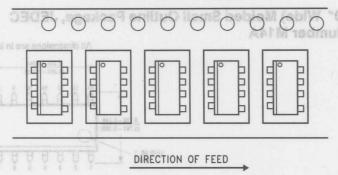
SMALLEST ALLOWABLE BENDING RADIUS.

TL/F/11642-10

Pkg Type	Tape Size	Dim A	Dim Ao	Dim B	Dim Bo	Dim F	Dim Ko	Rad R	Dim W
20 SO (200 mil)	24 mm	8.7	8.4	13.5	13.2	11.5	2.4	50.0	24.0
14/16 SO (200 mil)	16 mm	8.7	8.4	11.0	10.7	7.5	2.4	50.0	16.0

Tape and Reel Specifications and Drawings (Continued)

Direction of Feed for SOIC Devices



TL/F/11642-11

Tape and Reel Quantities

Package REAL OF THE PACKAGE PA	Qty of Sealed Devices
JEDEC 14/16	2500
JEDEC 20/24	1000
EIAJ 14/16/20	1000

JEDEC and EIAJ SOIC Carrier Tape Specifications

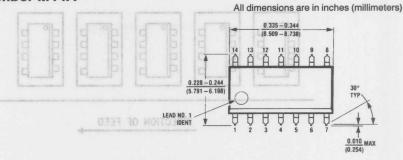
		Lead	er (mm)			Hub (mm)						
Unsealed Carrier		Sealed Carrier		E 25 E 126	Overall Carrier		Unsealed Carrier		aled rrier	[My 2017] [My 256 C	erall rrier	
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
0	400	500	1200	500	1200	0	340	300	640	300	740	

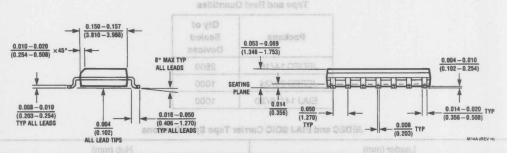
The overall carrier minimum specification is determined by the sealed carrier minimum.

The overall carrier maximum consists of the sealed carrier minimum plus a combination of unsealed carrier and any additional sealed carrier. For example, the leader's overall maximum of 1200 mm consists of a 500 mm minimum sealed carrier, with a remaining 700 mm combination of unsealed (0 mm to 400 mm) and/or sealed (0 mm to 700 mm) carrier.

The number of pockets in the leader or hub carrier tape are determined by the tape's pitch. For example the pitch for a JEDEC SOIC 14 (mil) 16 mm tape, the P1 dimension from the previous pages, is 8.0 mm. Thus the maximum leader unsealed carrier pockets would be 400 mm/8 mm or 50.

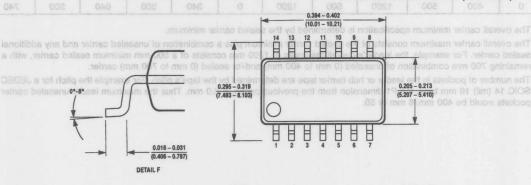
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M14A

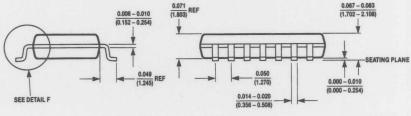




14 Lead Molded Small Outline Package (SOP), EIAJ Type II NS Package Number M14D

All dimensions are in inches (millimeters)

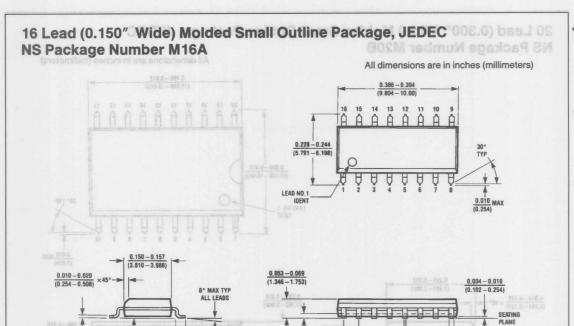




M14D (REV A)

0.014-0.020 TYP

(0.356 - 0.508)



0.014

(0.356)

(1.270)

0.008 (0.203) TYP

16 Lead Molded Small Outline Package (SOP), EIAJ Type II NS Package Number M16D

0.016 - 0.050

(0.406 - 1.270)

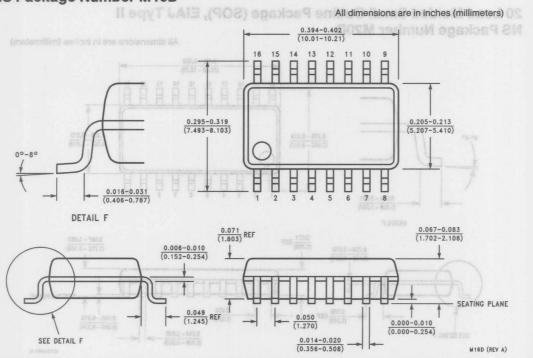
0.008-0.010

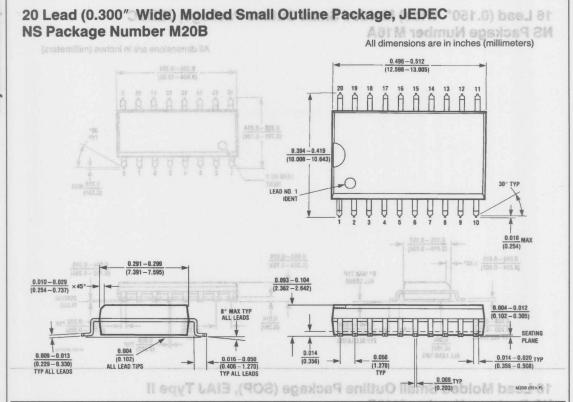
(0.203 - 0.254)

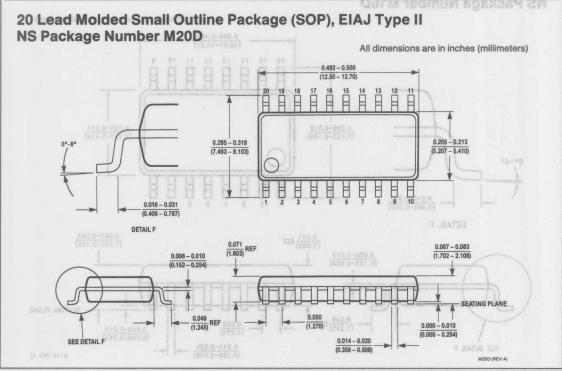
TYP ALL LEADS

0.004

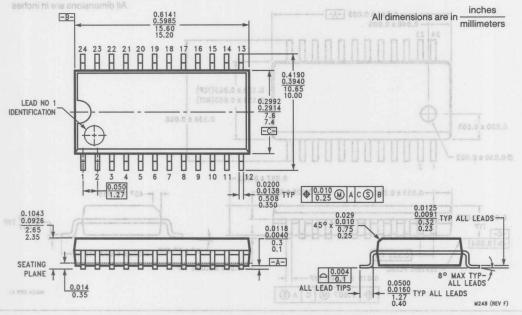
(0.102) ALL LEAD TIPS



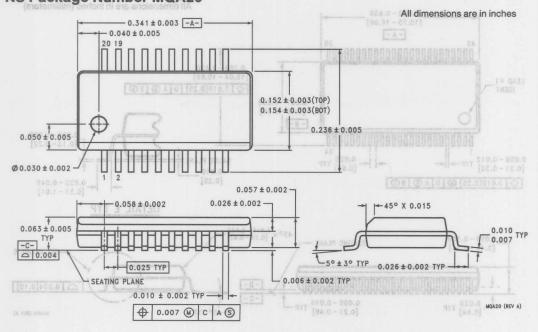


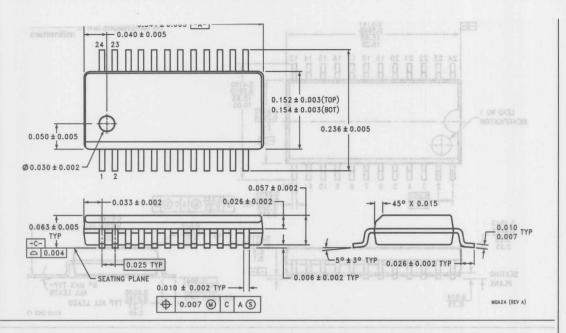




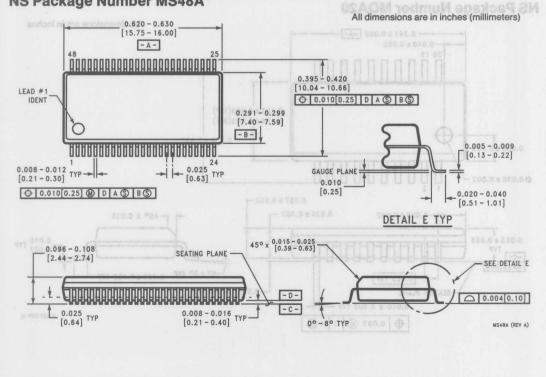


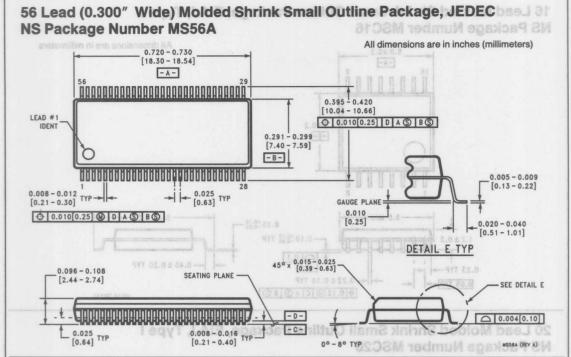
20 Lead (0.150" Wide) Molded Shrink Small Outline Package, JEDEC NS Package Number MQA20



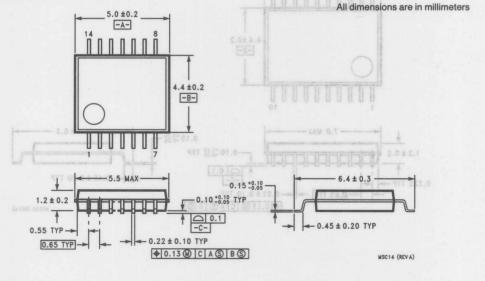


48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC NS Package Number MS48A

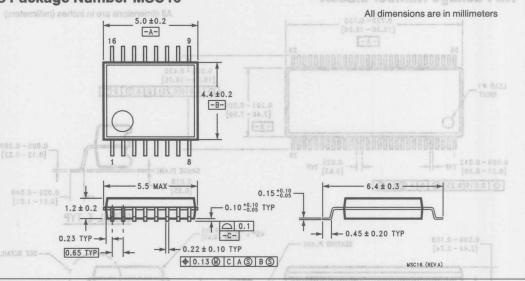




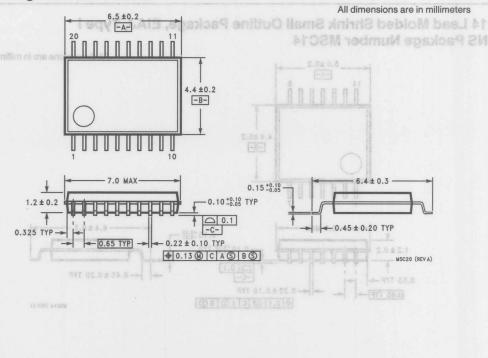
14 Lead Molded Shrink Small Outline Package, EIAJ, Type I NS Package Number MSC14

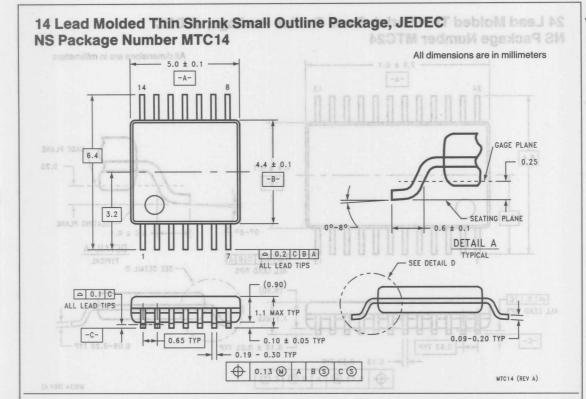


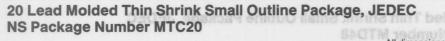
16 Lead Molded Shrink Small Outline Package, EIAJ, Type I 1008.0) bas J 33 NS Package Number MSC16

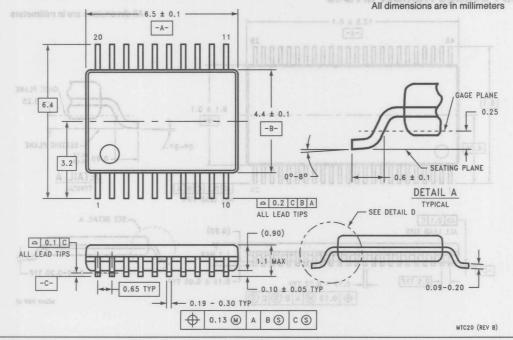


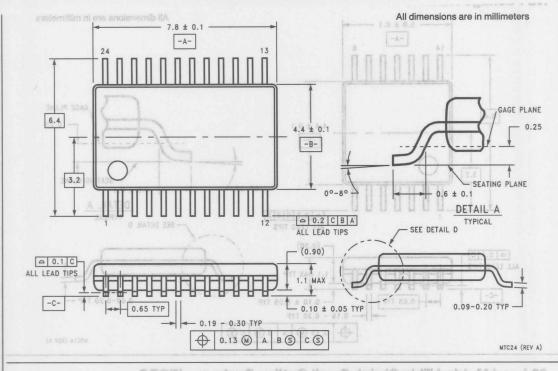
20 Lead Molded Shrink Small Outline Package, EIAJ, Type I NS Package Number MSC20











48 Lead Molded Thin Shrink Small Outline Package, JEDEC NS Package Number MTD48

